The Impacts of BSIM

Sally Liu

TSMC

Dec 13, 2012

The Impacts of BSIM

- Outline
  - What is BSIM
  - Industry standard
  - Breadth and depth
  - Moving forward

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What’s in a name of BSIM

- The making of BSIM
  - 631 papers in IEEE Explore database by Hu’s team
    - Modeling HC, BV, PT … etc in late ‘70 and early ‘80
    - 1984: 1st paper on IGFET charge model
  - “BSIM” was coined in 1987

Berkeley Short-channel IGFET Model

- The BSIM family
  - BSIM, BSIM1-6 – planar MOSFETs
  - BSIM-MG, BSIM-CMG, BSIM-IMG – 3D FinFETs
  - BSIMSOI, BSIMPD, BSIM-IMG – SOI MOSFETs

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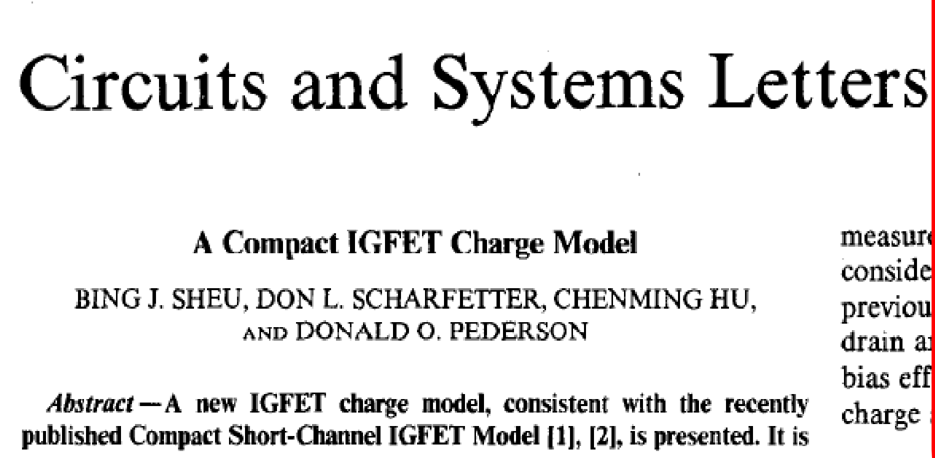
BSIM was born



IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, VOL. CAS-31, NO. 8, AUGUST 1984

Circuits and Systems Letters

A Compact IGFET Charge Model

BING J. SHEU, DON L. SCHARFETTER, CHENMING HU,
AND DONALD O. PEDERSON

Abstract—A new IGFET charge model, consistent with the recently published Compact Short-Channel IGFET Model [1], [2], is presented. It is

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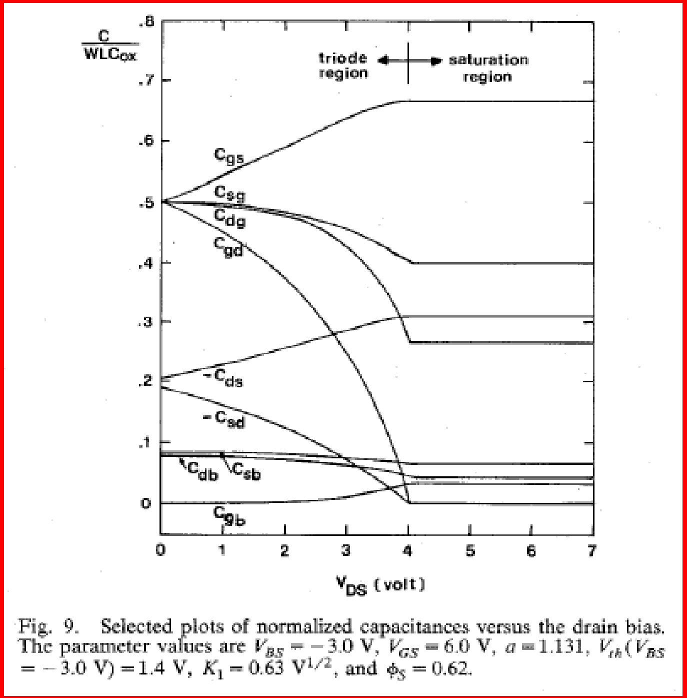


Fig. 9. Selected plots of normalized capacitances versus the drain bias. The parameter values are $V_{BS} = -3.0$ V, $V_{GS} = 6.0$ V, $a = 1.131$, $V_{th}(V_{BS} = -3.0\ \text{V}) = 1.4$ V, $K_1 = 0.63\ \text{V}^{1/2}$, and $\phi_S = 0.62$.

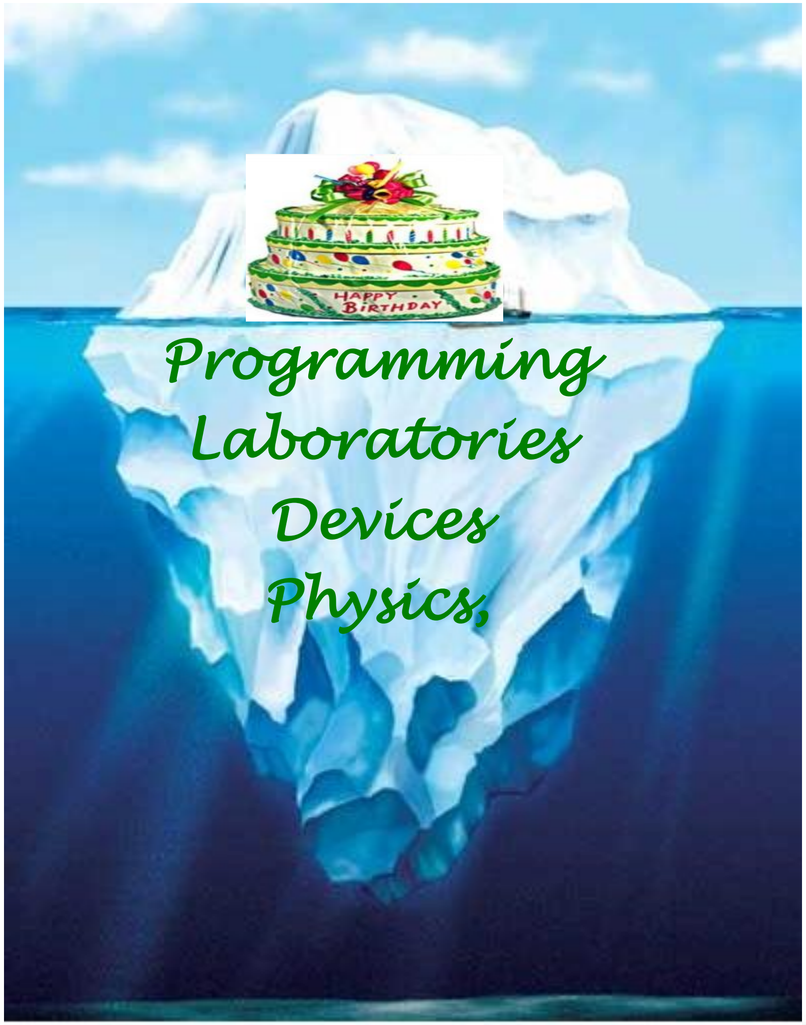
558 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-22, NO. 4, AUGUST 1987

BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors

BING J. SHEU, MEMBER, IEEE, DONALD L. SCHARFETTER, FELLOW, IEEE, PING-KEUNG KO, MEMBER, IEEE,
AND MIN-CHIE JENG

Tip of an iceberg

- One team
  - Physics
  - Devices
  - Laboratories
  - Programming
- Academia & industries
  - Evaluations / benchmarking
  - Enhancements / extension
  - Applications / validation



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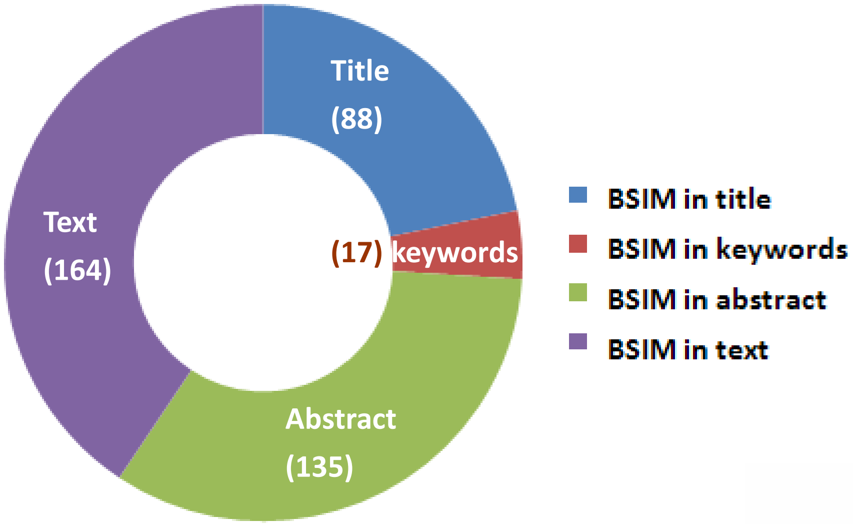
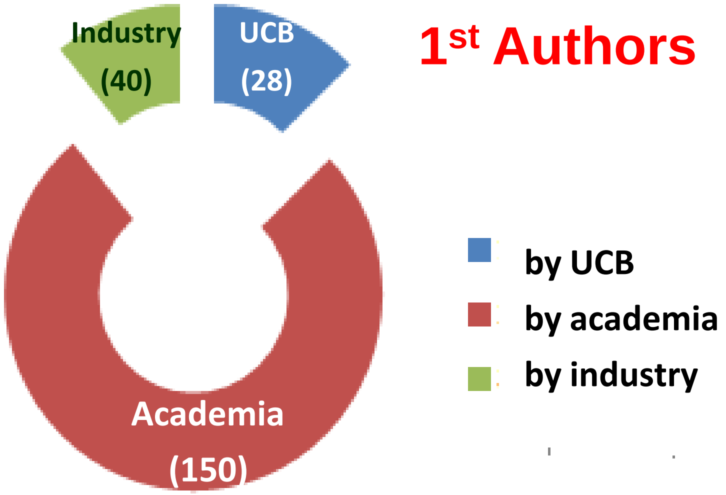
Let the BSIM numbers speak

- **More than 200 "BSIM" articles**
    - IEEE Explore Database

Honorable mentions



1st Authors



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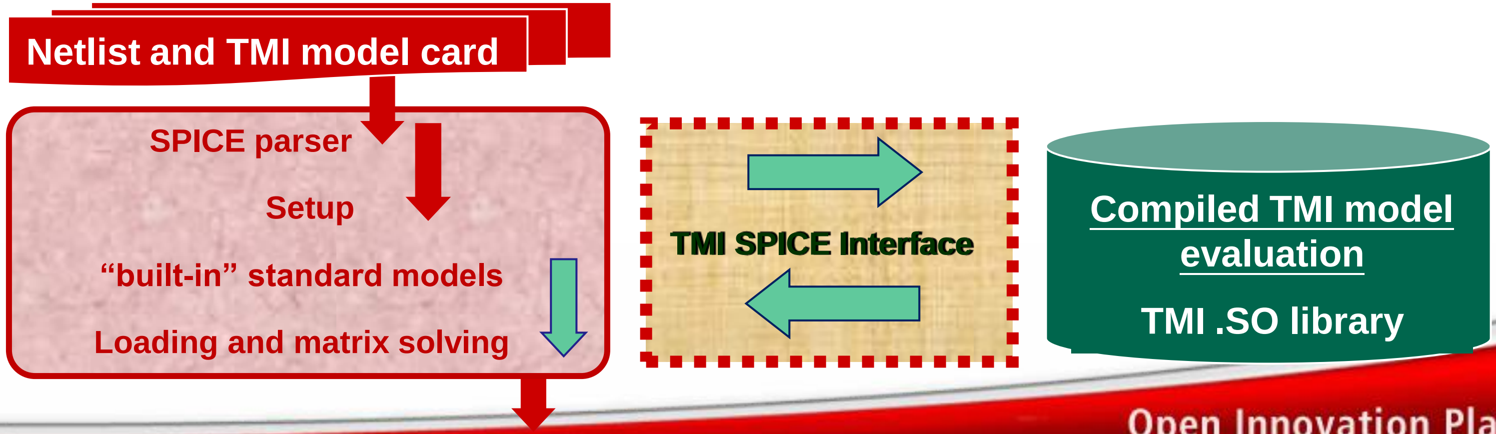
The BSIM standard – the beginning

- Compact model council (CMC) started before 1996
  - In a time of fragmented compact model development
    - Though, "de facto standard" MOSFET model exists
    - Different flavored models in alphabet SPICE's
    - IDM's have their proprietary models & tools
    - Cross team design hand-shakes were chaotic
- BSIM3v3 elected as the first CMC standard model
  - Extensive benchmarking with cross industrial collaboration
  - BSIM team's dedication is key to its acceptance
- BSIM4 (2000), BSIMSOI (2002), BSIM-CMG(2012)
  - Critical nanometer effects
  - Emerging new device structures

The BSIM standard – now and future

- BSIM4 : the first CMC standard models in TMI2
  - TMI2: the first CMC application program interface (API),2010
    - HSPICE (SNSP), Spectre (CDS), Eldo (MGC)
- TMI2 API enables efficient macro modeling
  - Macro modeling = intrinsic device + extrinsic effects
    - Layout dependent effects, aging effects, restrict design rules
  - Proven efficiency in setup time, memory usage & computing



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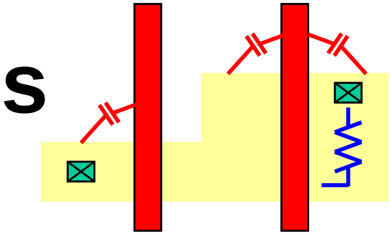
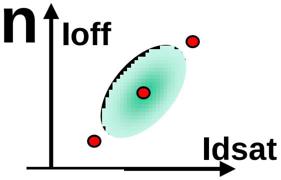
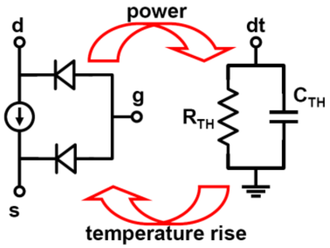
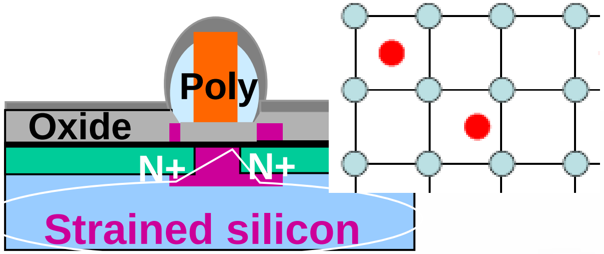
Macro modeling at nanometers

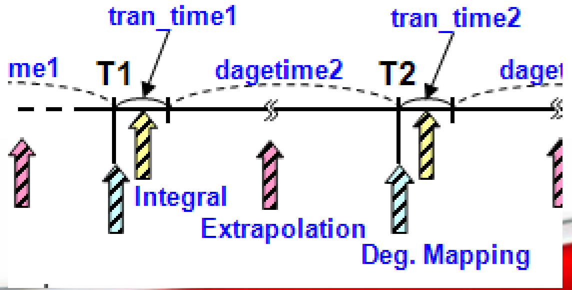


- Complex layout dependency – mechanical stress
- Middle layer (MEOL) effects – device local connects
- Restricted design rules for DFM – new lithography
- Statistical & parametric variations – local & global
- Self-heating effects – a node of device temperature
- Aging effects – age extrapolation & degradation
- Additional geometric scaling – half node …









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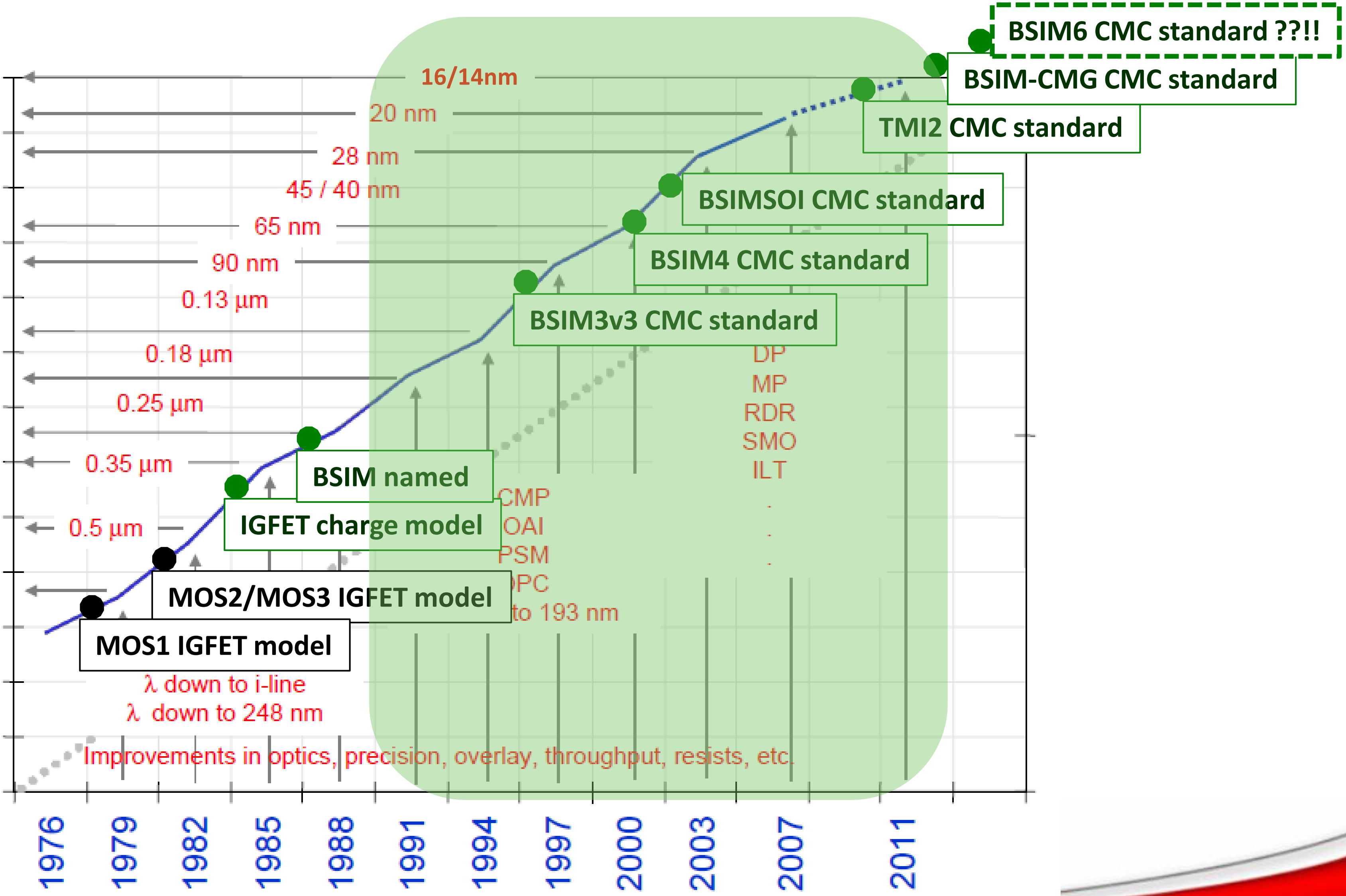
BSIM locomotive



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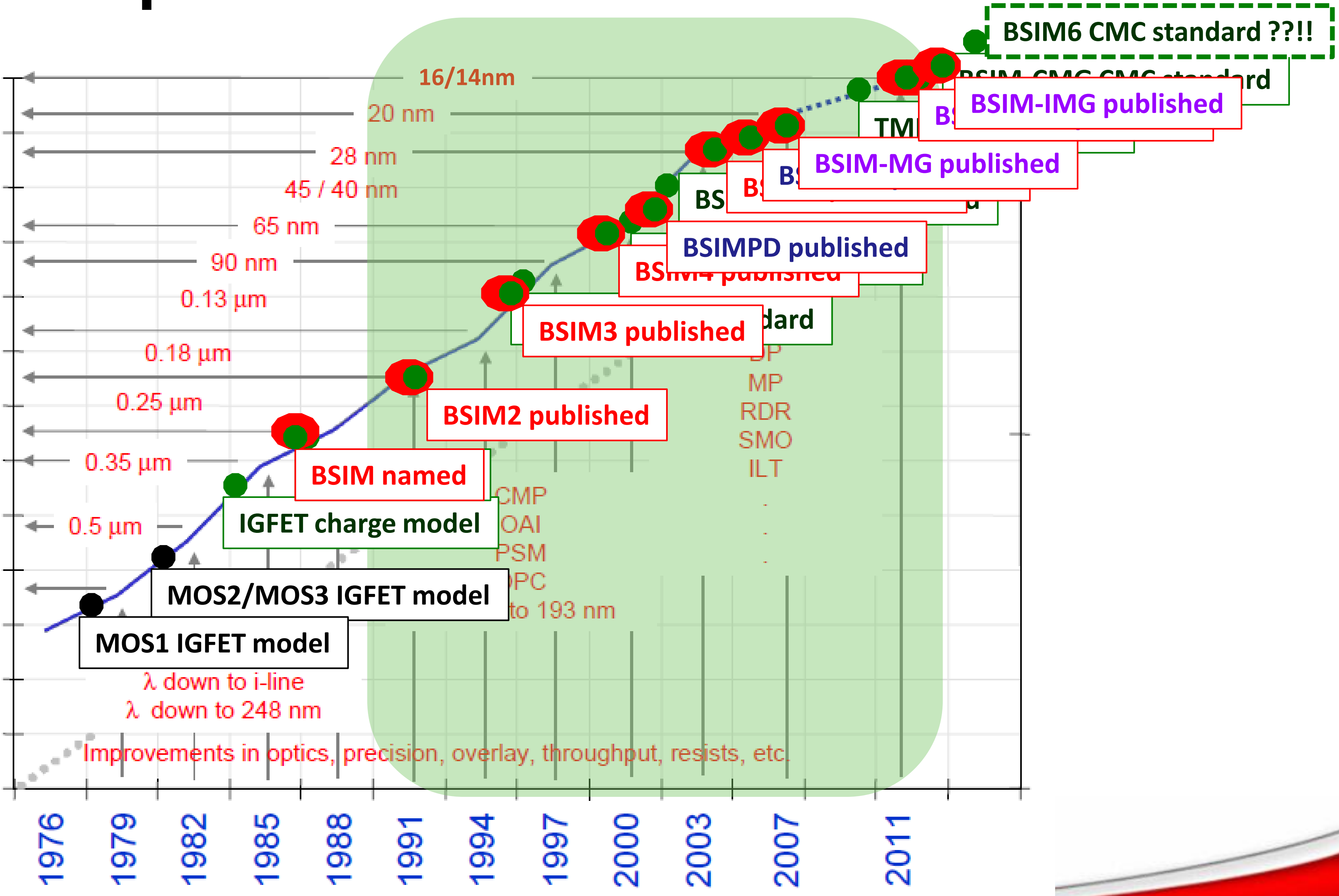
TSMC Property

BSIM portfolio



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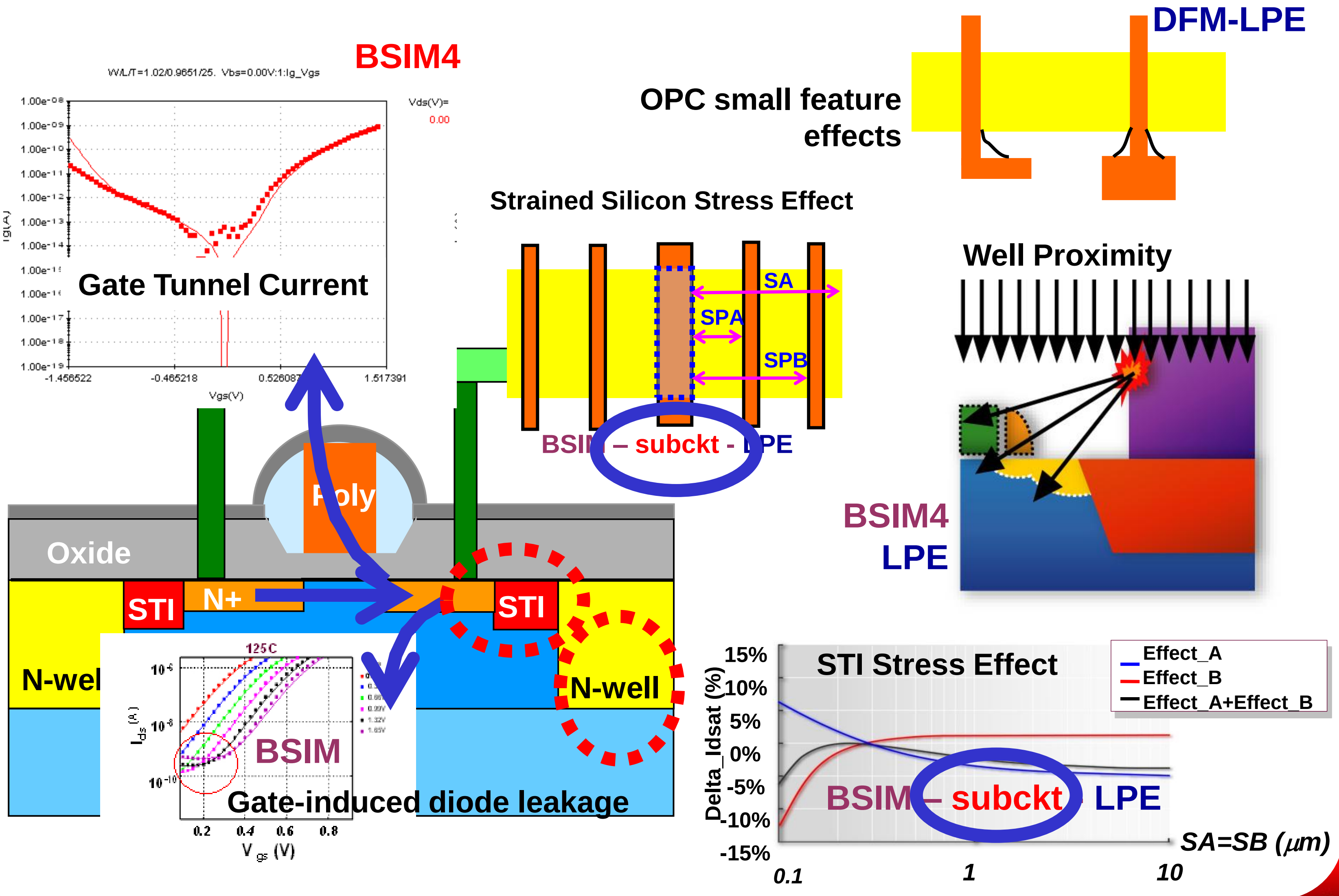
TSMC Property

BSIM4 critical features for nanometer



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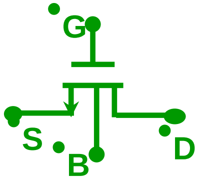
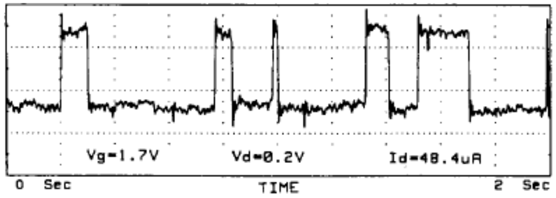
Required basic model features

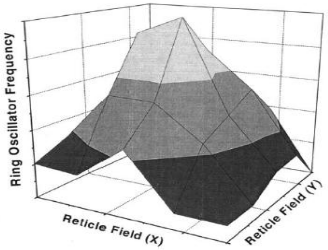


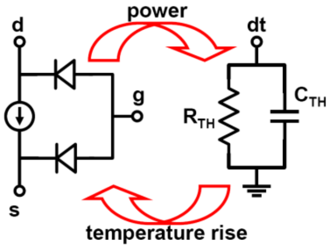
- Physical and accurate in inversion & accumulation regions
- Relevant small-geometry effects
- Relevant nanometer effects, e.g. halo implant, well-proximity, strained-silicon, shallow-trench stress, … etc
- Mobility modulation effects, e.g. velocity saturation, Coulomb scattering … etc
- Quantum-mechanical corrections
- Poly-depletion effects, gate-tunneling & hot-carrier leakage
- Non-quasi saturation (NQS) effects
- Charge /capacitance models conserving electric charge
- Noise models, including flicker and thermal

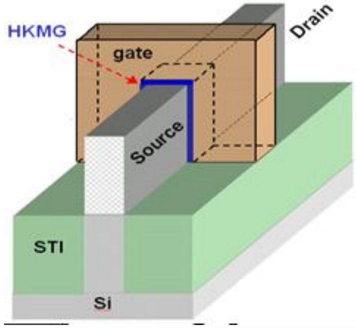
Emerging effects in deep nanometer

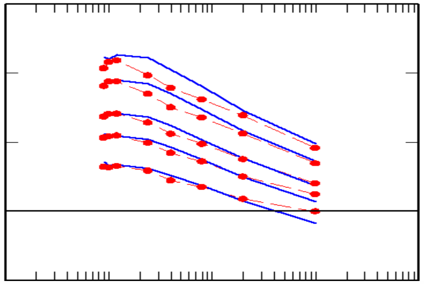
- New device structures – FinFET …
- Influence from device environment
- Scaling slope changing …
- Process variation of larger percentage
- Random telegraph noise
- Self heating
- Aging effects

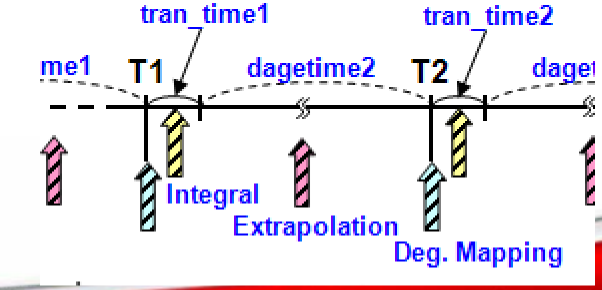












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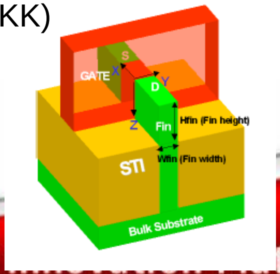
Evolution and revolution

- Foundry deployment
  - 2003: Gate tunneling current in BSIM4.3 (90nm)
  - 2004: STI stress & trap-assisted diode leakage in BSIM4.4
  - 2005: WPE in BSIM4.5 (65nm)
  - 2007: Composite STI stress by subckt macro (45/40nm)
  - 2008: More new LDE by subckt macro (28/20nm)
  - 2011: Aging model & FinFET model in TMI2 for beta testing
- Inventing FinFET

IEDM 1998: "A Folded channel MOSFET for Deep-sub-tenth Micron Era",

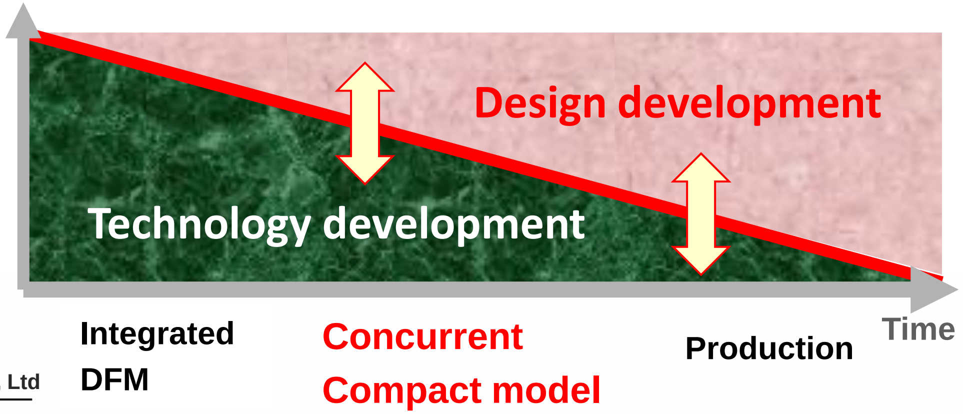
Digh Hisamoto, Wen-Chin Lee, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Kazuya Asano, Tsu-Jae King, Jeffrey Bokor, Chenming Hu (Hitachi, UCB, Lawrence Berkeley Lab, Nippon Steel, NKK)

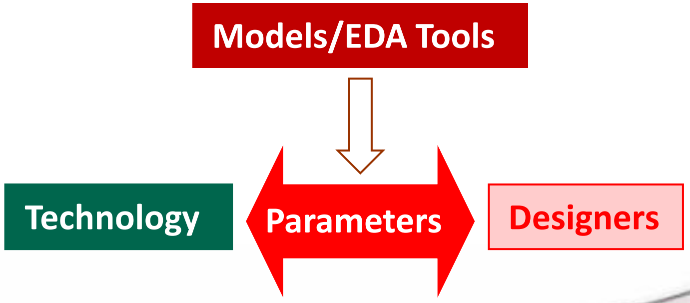
  - The viable transistor in sub-20nm
  - BSIM-CMG 106.0.0 now a CMC standard model



The deep-nano and post-silicon

- Compact models is pivotal in design enablement
  - More intensive collaboration between foundry & design
  - Early waves starts earlier
- Standard model and standard API key to deployment
  - Standard models definitely for device intrinsic behaviors
  - Macro-modeling definitely for surrounding influences





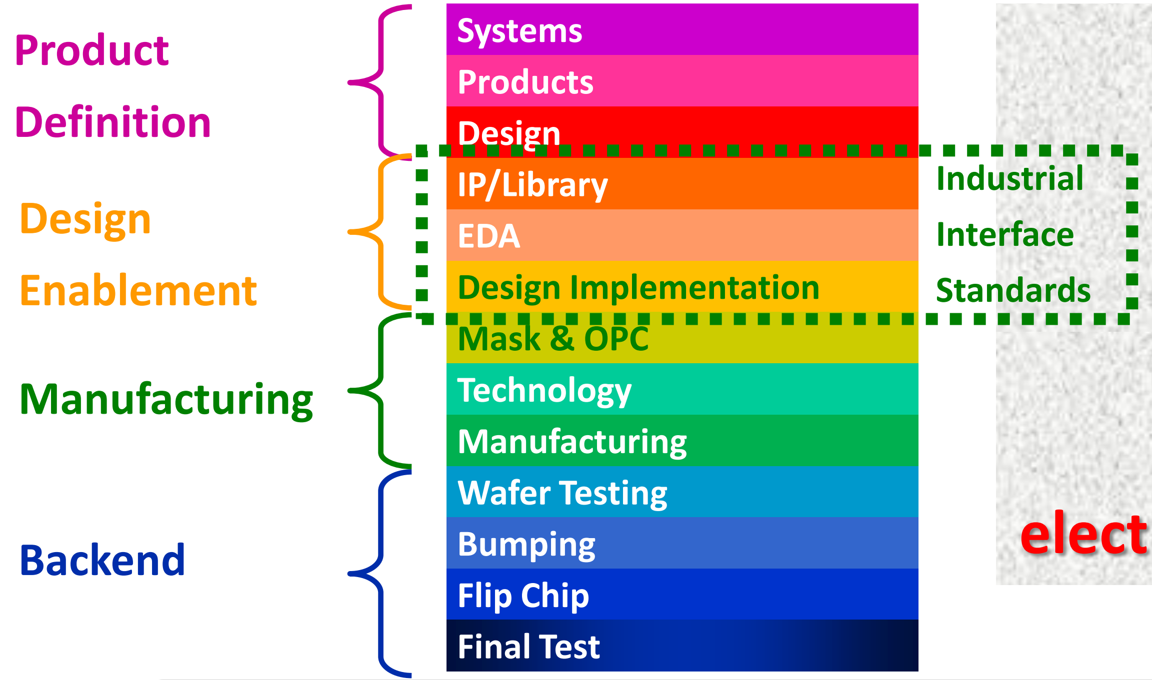
Models/EDA Tools

Technology

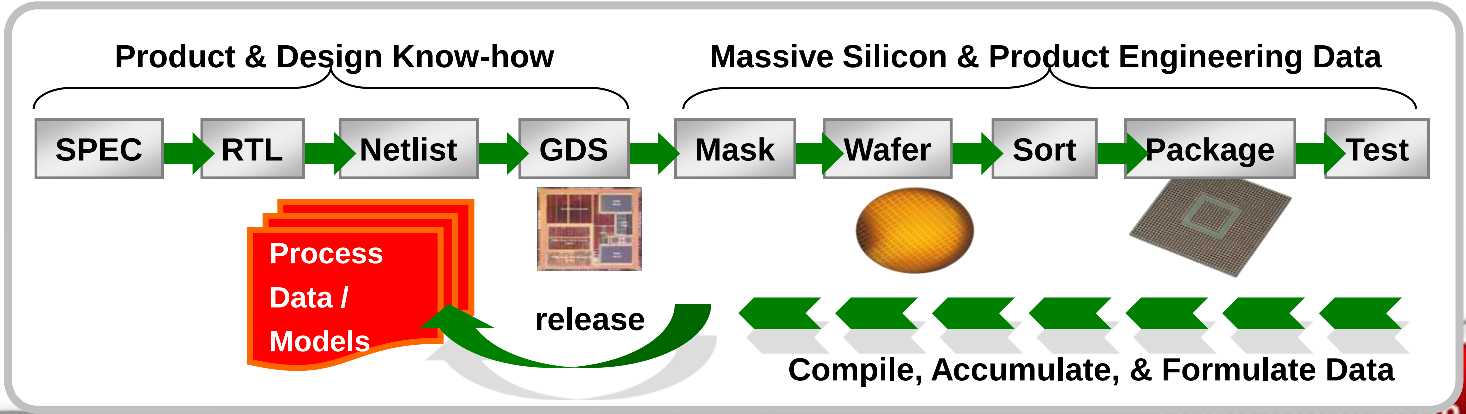
Parameters

Designers

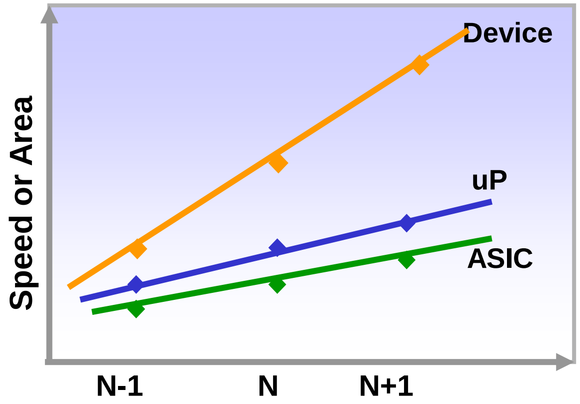
Semiconductor eco-system



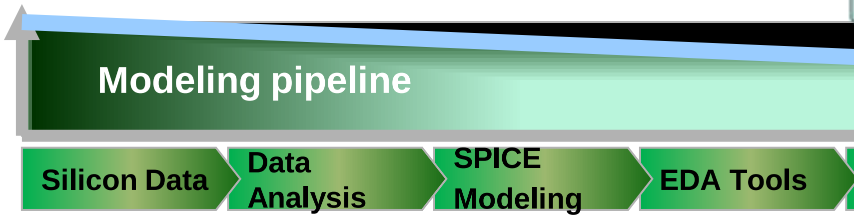
Compact model and parameters are the critical link in electrical information flow



The best yet to come



"ET" delivers performance, manufacturability, reliability in scaled dimensions

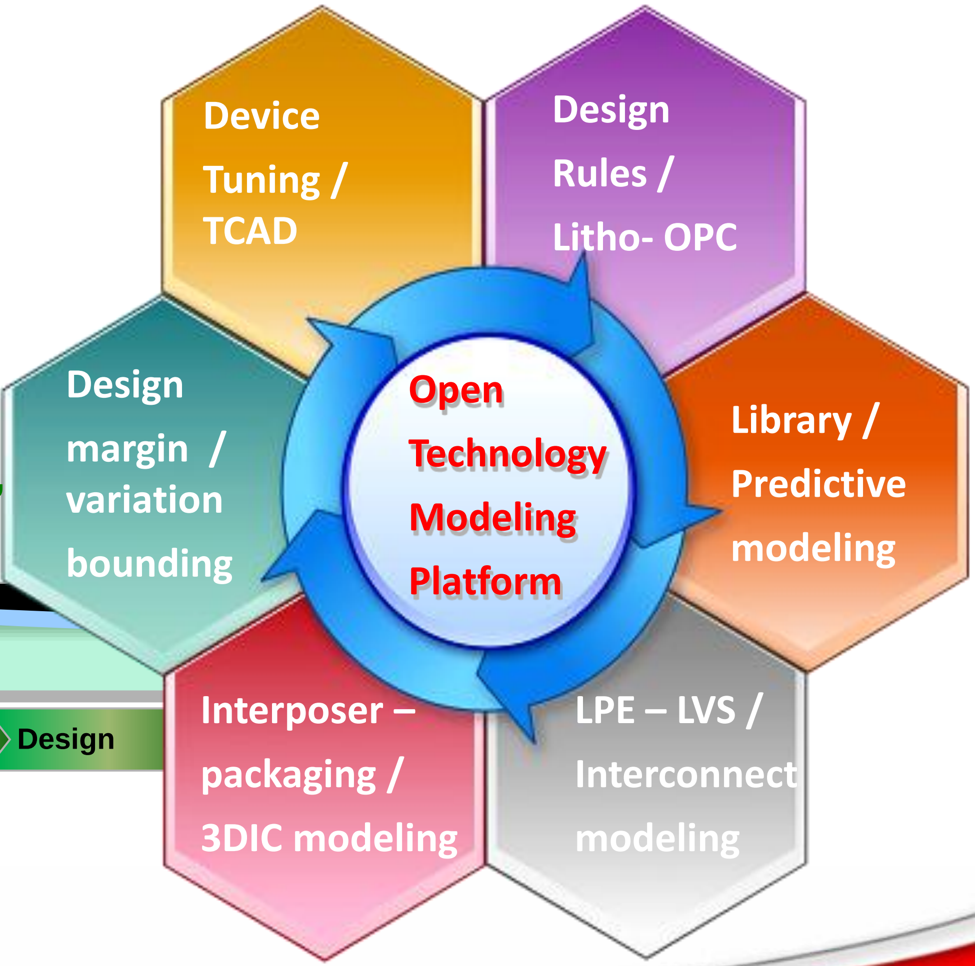


Modeling pipeline

Silicon Data → Data Analysis → SPICE Modeling → EDA Tools → Design

- ☐ "New / Changes" is the norm
  - ✓ New devices, new materials, new litho, new constraints,
  - ✓ Rapid recipe changes as ET evolves / revolves

An Eco-System for Innovations



Device Tuning / TCAD

Design Rules / Litho- OPC

Design margin / variation bounding

Open Technology Modeling Platform

Library / Predictive modeling

Interposer – packaging / 3DIC modeling

LPE – LVS / Interconnect modeling

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Acknowledgements

Dr. Min-Chie Jeng

Dr. Bing J. Sheu

Dr. K.W. Su

Dr. C.K. Lin

and members of TSMC Technology Modeling Division

for their assistance in the preparation and their contribution in advancing compact models at foundry