Semiconductor Manufacturing

Enabling Core Technologies

Chief Technology Officer

Silicon Systems Group

Applied Materials

UC Berkeley “Electrons to Electronics”

December 13, 2012

Key Themes

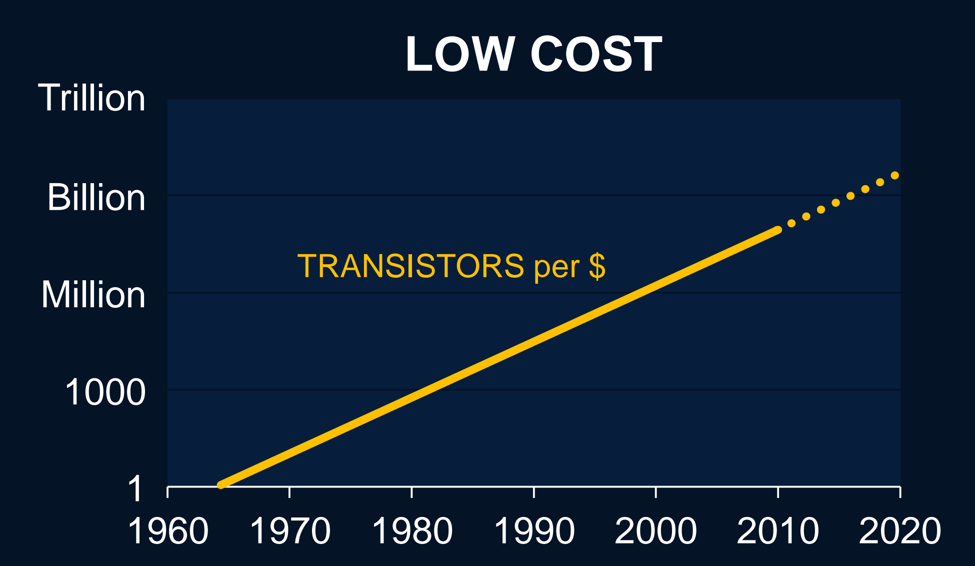
Mobility driving market and technology landscape

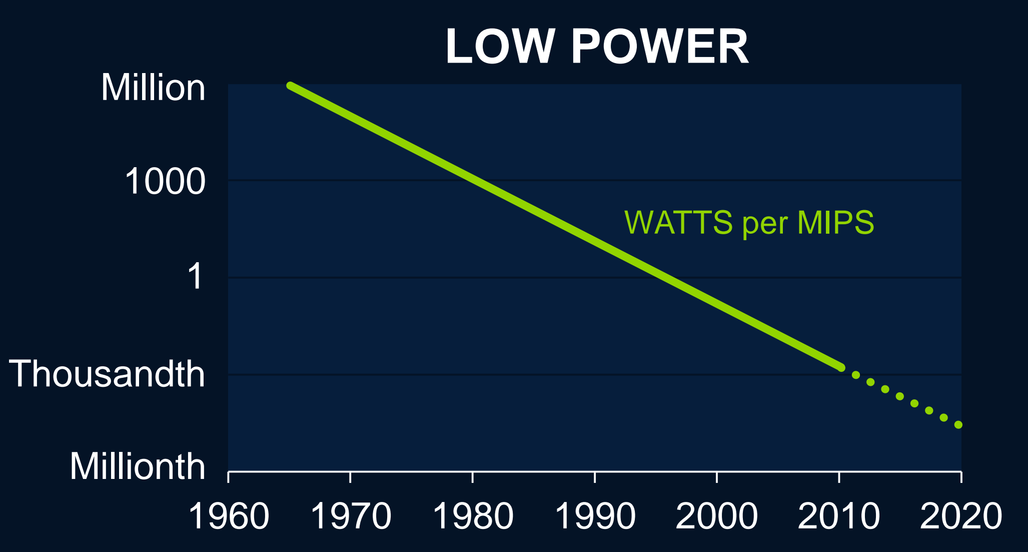
Cost is becoming the challenge

Increasing complexity – architectures, films, patterning

Technology and economics drives concentration

External Use





The Mobility **ERA**

External Use

The Cost Challenge

- Capital intensity
- Die cost (¢/mm²)
- R&D cost

- New business models
- Growth
- Deep profit pools

amazon.com

- Concentration
- Market leaders
- Volume

- Consolidation
- Many R&D paths

How to create certainty amid a diversity of solutions?

Logic/Foundry Roadmap

	2011	2013	2015	2017	2019	2021	2023
Node (nm)	22	14	10	7	5	3.5	2.5
Interconnect CD (nm)	40	30	20	15	10	7.5	5

Wafer Scaling
- 300mm
- 450mm

Transistor
- FinFET
- Nanowire
- SiGe
- III-V or III-V Tunnel FET

Interconnect
- Dual Damascene
- Single Damascene
- Subtractive Copper/Alternatives

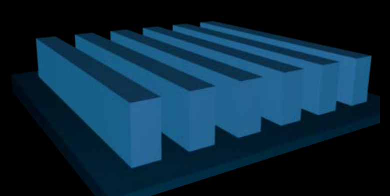
Embedded Memory
- SRAM
- MRAM

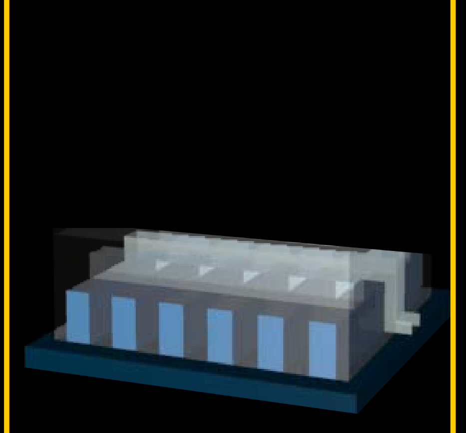
Patterning
- Immersion Multi Patterning
- Self-Assembly/ Vertical Device
- EUV

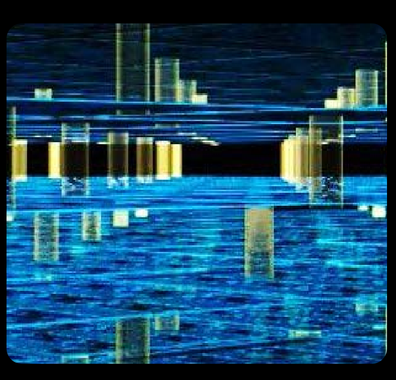
Required product capabilities

- Advanced Epi
- Advanced Dielectrics
- Interface engineering
- Advanced metals
- Materials Removal
- Pattern Integrity Solutions
- Patterning & Inspection <10nm

External Use







Advanced Patterning

Advanced Transistor

Advanced Interconnect

Wafer-Level Packaging

External Use

New Materials and New Structures Needed

Planar CMOS

FinFET

III-V FinFET

Nanowires

Gate

Silicon Substrate

Gate

Fin

STI Oxide

Silicon Substrate

New Fin Material

STI Oxide

Silicon Substrate

INCREASING (MATERIALS ARCHITECTURE INTEGRATION) COMPLEXITY

External Use

FinFET Parasitic Control

Dual Gate Thickness Control

Contact fill for <7nm contact width
- Thin liner
- Void free fill
- CMP

Metal Gate WF as fill
- Conductive nWF, pWF
- Dielectric gate cap

Miller Capacitance
- Dielectric mold for stressor

Silicide Rc reduction
- Integrated silicide preclean
- Metal/semi interface
- Barrier height modification

Lower K Dielectrics

Fin Formation:
- Precision etch
- Structural integrity (collapse, erosion, thermal shock)
- Recess control
- Channel materials

Engineering the High-k Stack Layers

Source
Drain

2 nm

High-k
Interface Layer
Si

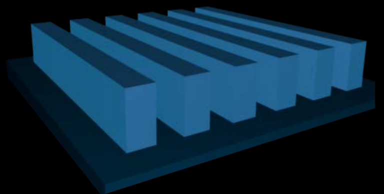
Atomic-scale engineering

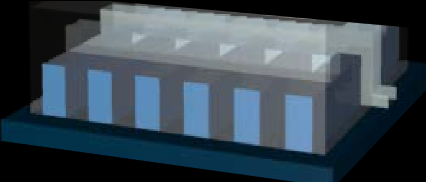
Material stability

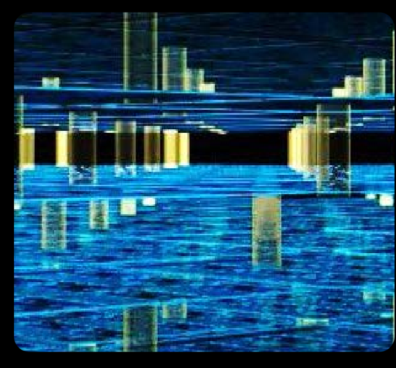
Interface layer precision

Source: Applied Materials Maydan Technology Center

External Use







Advanced Patterning

Advanced Transistor

Advanced Interconnect

Wafer-Level Packaging

External Use

Interconnect Challenge: RC-Delay

RC Delay Outlook

RC Delay (ns/mm): 0, 10, 20, 30, 40, 50, 60, 70, 80

Conventional

Technology Node: 32nm, 22nm, 15nm, 11nm

Conventional

- Blok
- Cap
- Low-k Dielectric
- Copper

RC-delay increase is driven by resistance component

External Use

Interconnect Improvement: RC-Delay

RC Delay Outlook

Disruptive

Solution requires new materials, architectures and tolerances

External Use

Focus Areas for Research

- Core Technology
  - Energy sources
  - Chemical delivery systems & chemistries
  - E-beam
  - Variability management
- Materials
  - Screening methods
  - Alternative materials: Graphene, Metal Oxide, III-V, optical
- Devices
  - 100mV switches
  - High packing density logic
  - Alternate channel, Optical interconnect, Interposer
- EUV Lithography

External Use

Complexity

Concentration

Collaboration

External Use

Turning innovations
into industries.™