Prospects for High-Aspect-Ratio FinFETs in Low-Power Logic

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High Aspect Ratio Fins for Low-Power Logic

*Fin thickness defined by Atomic layer epitaxy → nm thickness control*

*Fin height defined by sidewall growth → 200 nm high fins*

Enables ~4 nm fin bodies → 8 nm gate length
10:1 more current per unit die area
→ smaller IC die area
    complements lithographic scaling

Enables high speed, ultra low-power logic,
$V_{dd}$~300 mV

InGaAs finFET: 8 nm thick fin 200 nm high

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height>> pitch
Background: III-V MOS

V. Chobpattana et al (Stemmer group), APPLIED PHYSICS LETTERS 102, 022907 (2013)

$L_g = 60$ nm

$V_{DS} = 0.1$ to $0.7$ V
0.2 V increment

$G_m$ (mS/µm)

$V_{DS} = 0.1$ to $0.7$ V
0.2 V increment

$V_{GS} = -0.4$ V to $1.0$ V
0.2 V increment

$R_{on} = 268$ Ohm-µm
at $V_{GS} = 1.0$ V

SS ~ 80 mV
$V_{DS} = 0.1$ V
SS ~ 120 mV
$V_{DS} = 0.5$ V

Current Density (mA/µm)

Drain Bias (V)
FinFETs by Atomic Layer Epitaxy: Why?

**Electrostatics:**
body must be thinner than $\sim L_g / 2$
→ less than 4 nm thick body for 8 nm $L_g$

**Problem:**
threshold becomes sensitive to body thickness

$$\delta V_{th} \propto \delta T_{body} / T_{body}^3$$

**Problem:**
low mobility unless surfaces are very smooth

$$\mu \propto T_{body}^6 / \delta T_{body}^2$$

**Implication:** At sub-8-nm gate length, need:
atomically-smooth interfaces
atomically-precise control of channel thickness

side benefit: high drive current → low-voltage, low-power logic
ALE-Defined finFET: Process Flow

**Fin template:** formed by \{110\}-facet-selective etch → atomically smooth

**Channel thickness set by ALE growth** → atomically precise

*Not shown: gate dielectric, gate metal, S/D metal*
Images

- HfO$_2$
- fin, $\approx 8\text{nm}$
- TiN

50 nm fin pitch

10 nm thick fins, 100 nm tall

100 nm fin pitch

source
channel

20 nm

200 nm
Goal: Tall Fins for High Drive Current

\[
\frac{\text{current}}{\text{transistor width}} = J_{\text{surface}} \cdot \frac{\text{fin height}}{\text{fin pitch}}
\]

Goal: fin height $\gg$ fin pitch (spacing) $\rightarrow$ more current per fin
$\rightarrow$ less fins needed $\rightarrow$ higher integration density

Higher density $\rightarrow$ shorter wires $\rightarrow$ smaller $C_{\text{wire}}V_{\text{dd}}/I$, $C_{\text{wire}}V_{\text{dd}}^2/2$
Is the IC Area Reduction Significant?

Clock/interconnect drivers need large drive currents. Area reduction for these is likely substantial.

FETs in Cache Memory & Registers are drawn at minimum width. No area reduction for these.

Most, but not all, Logic Gates will be drawn at minimum width.

Benefit must be evaluated by VLSI architect, not by device physicist.
300 mV Logic: Can We Address The $CV^2/2$ Limit?

**The $CV^2/2$ dissipation limit**

![Graph showing $I_d$ vs $V_{gs}$ for $V_{dd}$ set for target $I_{on}$, hence acceptable $CV_{dd}/I_{on}$. Threshold set for acceptable off-state dissipation $I_{off}V_{dd}$.]

$V_{dd}$ is set for target $I_{on}$, hence acceptable $CV_{dd}/I_{on}$. Threshold set for acceptable off-state dissipation $I_{off}V_{dd}$.

With minimum $C_{wire}$, a minimum switching energy $C_{wire}V_{dd}^2/2$ is set.

**Subthreshold logic**

![Graph showing $I_d$ vs $V_{gs}$ for $V_{dd}$ is simply reduced. Decreases energy $CV_{dd}^2/2$. Increases delay $CV_{dd}/I_{on}$.]

$V_{dd}$ is simply reduced.
Decreases energy $CV_{dd}^2/2$.
Increases delay $CV_{dd}/I_{on}$.

**Tunnel FETs**

![Diagram of Tunnel FETs showing source, gate, dielectric, drain, P+ source, channel, N+ drain, and barrier.]

Bandgap of P+ source truncates thermal distribution.

Potential for low $I_{off}$ at low $V_{dd}$.

Obtaining high $I_{on}/V_{dd}$ is the challenge.
Goal: Tall Fins for Low-Power, Low-Voltage Logic

Supply reduced from 500mV to 268 mV while maintaining high speed.

3.5:1 power savings? Must consider FET capacitances.

Assumes (Hodges & Jackson, 2003): (1) Charge-control analysis  
(2) \( I_{on,PFET} / W_g = 0.5 * I_{on,NFET} / W_g \)  
(3) FO=FI=1
Power and Delay Comparison

**Planar FET, \( V_{dd} = 500 \text{ mV} \)**

- \( I_{on} = 20 \mu A, \ I_{off} = 2nA \)
- \( C_{g-ch} = \frac{I_{on} L_g}{V_{inj} V_{dd}} = 1.3 \text{ aF} \)
- \( C_{gd-f} = C_{gs-f} = 6 \text{ aF} \)
- \( C_{wire} = 2 \text{ fF (10 \mu m length)} \)
- \( C_{total} = 2.1 \text{ fF (various multipliers)} \)
- \( \text{delay} = 52 \text{ ps} \)
- \( C_{total} V_{DD}^2 = 0.26 \text{ fJ} \)

**tall finFET, \( V_{dd} = 268 \text{ mV} \)**

- \( I_{on} = 20 \mu A, \ I_{off} = 2nA \)
- \( C_{g-ch} = \frac{I_{on} L_g}{V_{inj} V_{dd}} = 3.7 \text{ aF} \)
- \( C_{gd-f} = C_{gs-f} = 60 \text{ aF} \)
- \( C_{wire} = 2 \text{ fF (10 \mu m length)} \)
- \( C_{total} = 2.9 \text{ fF (various multipliers)} \)
- \( \text{delay} = 39 \text{ ps} \)
- \( C_{total} V_{DD}^2 = 0.11 \text{ fJ} \)
Why tall finFETs? Why Not Just Subthreshold Logic?

Planar FET, $V_{dd} = 268 \text{ mV}$

$tall \text{ finFET, } V_{dd} = 268 \text{ mV}$

Low $I_{on} \rightarrow large CV_{DD}/I_{on}$ delay, subthreshold logic is slow.

$I_{on} = 2.0 \mu A$

$I_{on} = 20 \mu A$
Why tall finFETs? Why Not Just Subthreshold Logic?

**Planar FET,** \( V_{dd} = 268 \text{ mV} \)

\[ I_{on} = 20 \mu\text{A} \]

**tall finFET,** \( V_{dd} = 268 \text{ mV} \)

**Die size increased 10:1**

(also: longer interconnects, etc)

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Tunnel FETs & High-Aspect-Ratio Fins

Quick performance estimate:
Assume, for a moment, that P/N tunneling probability is 10%.*
Typical of the best reported ohmic contacts.*

Then on-currents for tunnel FETs are ~10:1 smaller than that of normal FETs.

Unless $I_{on}/W_g$ is high, tunnel FETs will suffer from either
large $C_{wire}V/I$ gate delays or (increasing FET widths) large die areas.

Using high-aspect ratio fin structures, tunnel FET drive currents can be increased.
Parasitic fringing capacitance will then also contribute to $CV/I$ & $CV^2$.

*Contact to N-InGaAs @ 6E19/cm³ doping: $m^*=0.1m_0$, 0.2 eV, 0.5 nm barrier
**finFETs Defined by Atomic Layer Epitaxy**

*InGaAs finFET:*
- 8 nm thick fin
- 200 nm high

**Benefits:**
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- Enables high speed, ultra low-power logic,
  $V_{dd} \sim 300$ mV

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