Sub-Boltzmann Transistors with Piezoelectric Gate Barriers

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29 Oct, 2013
OUTLINE

❖ Motivation: Power dissipation in FET devices & circuits

❖ Existing ideas on steep slope FETs for low-voltage/low-power applications

❖ Negative Capacitance using electrostriction effect in a piezoelectric gate barrier (Novel Idea) - Design of sub-60mV/decade FET

❖ Conclusion
MOTIVATION: POWER CONSUMPTION

Power density evolution in Intel Processors!


Basic CMOS Unit:

\[ P \sim N(C V^2_d d + P_{off}) \]

- Large Static and dynamic power dissipation in large scaled ICs
- Large amount of heat generated in ICs
- Limits the scaling and computing Performance of ICs
Possible Solution: Steep Slope FET switch

Ideal switch SS ~ 0
60 mV/decade
<60 mV/decade

Allows further voltage $V_{dd}$
Scaling in ICs & reduce power dissipation

Subthreshold Slope:

$$SS = \frac{\partial V_{gs}}{\partial (\log_{10} I_d)} = \frac{\partial V_{gs}}{\partial \psi_s} \frac{\partial \psi_s}{\partial (\log_{10} I_d)} = m \times 60 \text{ mV/dec}$$

$E(eV)$

$$f(E - E_F) \sim e^{-E/kT}$$

Existing Ideas: 1) TFETs/I-MOS, 2) Negative capacitance using ferroelectric gate material (Internal voltage step up)

Need to modify these factors for < 60 mV/decade!
Subthreshold Slope:

\[ SS = \frac{\partial V_{gs}}{\partial (\log_{10} I_d)} = \frac{\partial V_{gs}}{\partial \psi_s} \frac{\partial \psi_s}{\partial (\log_{10} I_d)} = \left(1 + \frac{C_s}{C_{ins}}\right) \times 60 \text{ mV/dec} \]

Internal voltage gain:

\[ \frac{\partial \psi_s}{\partial V_{gs}} > 1 \]

SS < 60 mV/decade

Negative curvature of energy

Negative capacitance at free energy maxima

ELECTROSTRICTION IN PIEZOELECTRIC GATE BARRIER

Mechanism:
Electrostriction

External Applied Voltage

Piezoelectric Material (AlN)

Electric field-induced deformation of PE layer

Modulation of PE barrier thickness with applied bias:

\[ (t_{PE} - \Delta t_{PE}) \]

Voltage drop across the PE layer:

\[ V = \left(\frac{(\sigma_P + \sigma_{sp} \cdot \varepsilon_{33} \cdot \gamma_{33})/\varepsilon_{33}}{t_{PE} - \Delta t_{PE}}\right) \times \left(\frac{\sigma_P^2}{C_{33} \varepsilon_{33}}\right) \]

\[ \Delta t_{PE}/t_{PE} = \frac{\sigma_P^2}{C_{33} \varepsilon_{33}} \]

\[ \pm \frac{t_{PE}}{C_{33} \varepsilon_{33}^2} \cdot \sigma_P^4 - \frac{t_{PE}}{C_{33} \varepsilon_{33}^2} \cdot \sigma_P^3 + \left(\frac{t_{PE}}{C_{33} \varepsilon_{33}^2} \cdot \sigma_{sp}\right) \cdot \sigma_P^2 + \frac{t_{PE}}{\varepsilon_{33}^2} \cdot \sigma_P + \frac{t_{PE}}{\varepsilon_{33}^2} \cdot \sigma_{sp} - V = 0. \]

4th order non-linear charge equation
CHARGE STATES IN THE PIEZOELECTRIC LAYER

**Mechanism:**
- **Electrostriction**

**Charge states (Q2 & Q3)** (Negative capacitance)

**Charge state (Q1)** (Positive capacitance)

**Normal Charge state**

\[ Q = C_{geo} V \]

**Driving Force:**
- Large Field-Induced Deformation
- Strong Electromechanical Interaction
- Higher Piezoelectricity
- Higher Spontaneous Polarization

**Constant geometric capacitance**
ELECTROMECHANICAL CAPACITANCE

Capacitance vs. Voltage Curve

- Voltage-dependent capacitance for different charge states due to electrostriction in PE layer
  - Positive capacitance
  - Negative capacitance

Results in negative capacitance in the PE layer
Motivates to use as active gate barriers for Steep Slope FETs

Capacitance vs. Voltage Curve

- PE layer, AlN
- $\varepsilon_{33} = 9\varepsilon_0$
- $C_{33} = 373$ GPa
- $e_{33} = 1.55$ C/m²

$t_{PE} = 2.5$ A

$C_{geo} = \varepsilon_{33}/t_{PE}$
Change in free energy density in PE layer:

\[ H = \frac{1}{2} C_{ijkl} \gamma_{ij} \gamma_{kl} - \frac{1}{2} \epsilon_{ij} E_i E_j - e_{ijk} E_i \gamma_{jk} - E_i P \]

\[ \gamma_{zz} = - \frac{P_z^2}{(C_{33} \epsilon_{33})} \]

\[
\left( \frac{2 t_{PE}}{C_{33} \epsilon_{33}^2} \right) \cdot \sigma_P^3 + \left( \frac{3 e_{33} t_{PE}}{C_{33} \epsilon_{33}^2} \right) \cdot \sigma_P^2 \\
- \left( \frac{t_{PE}}{\epsilon_{33}} \right) \cdot \sigma_P - V = 0,
\]

\[ \sigma_P = C_{sc} \psi_s \]

\[ \alpha_3 \psi_s^3 + \alpha_2 \psi_s^2 - \alpha_1 \psi_s - (V_{gp} - \psi_s) = 0, \]

Device Structure:

Piezoelectric material: Active Gate barrier

Coefficients:

\[ \alpha_3 = \left( \frac{2 t_{PE}}{C_{33} \epsilon_{33}^2} \right) \cdot C_{sc}^3 \]
\[ \alpha_2 = \left( \frac{3 e_{33} t_{PE}}{C_{33} \epsilon_{33}^2} \right) \cdot C_{sc}^2 \]
\[ \alpha_1 = \left( \frac{t_{PE}}{\epsilon_{33}} \right) \cdot C_{sc} \]

Surface Potential vs. Gate Bias Voltage

Amplification of Surface Potential Relative to Gate Voltage

Subthreshold Slope (SS):

\[ SS = \frac{\partial V_{gs}}{\partial \psi_s} \frac{\partial \psi_s}{\partial (\log_{10} I_d)} \]

Body factor:

\[ m < 1 \]

\[ SS = m \times 60 \text{ mV/dec} \]

\[ SS < 60 \text{ mV/dec} \]
Transfer Curve

- Use of PE (AlN) gate barrier with NDC
- GaN channel HEMT
- Use of $\psi_s$-based Compact model
- Steep Subthreshold Slope $\sim 50$ mV/decade
OUTPUT CHARACTERISTICS

$I-V$ characteristics:

- Use of PE (AlN) gate barrier with NDC
- GaN channel HEMT
- Use of $\psi_s$-based Compact model
We showed NDC in a thin piezoelectric layer ($t_{PE} < 5$ nm) using electric field-induced electrostriction effect in the layer.

Proposed piezoelectric material as the *active* gate barrier for energy-efficient steep slope transistors.

Electrostriction & piezoelectricity internally amplify the channel surface potential over the applied gate bias voltage.

Showed internal voltage gain and *sub-60 mV/decade* subthreshold switching using Polar piezoelectric barrier.

Model for an AlN barrier in the GaN channel HEMT predicts *50 mV/decade* subthreshold slope.
Acknowledgement

• LEAST Program, and Director Prof. Alan Seabaugh

Thank You for your Attention!