Sub-Boltzmann Transistors with Piezoelectric Gate Barriers

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OUTLINE

- ❖ Motivation: Power dissipation in FET devices & circuits
- ❖ Existing ideas on steep slope FETs for low-voltage/low-power applications
- ❖ Negative Capacitance using electrostriction effect in a piezoelectric gate barrier (Novel Idea) - Design of sub-60mV/decade FET
- ❖ Conclusion

MOTIVATION: POWER CONSUMPTION

Power density evolution in Intel Processors !

Sun's surface (6 kW/cm²)

Nuclear reactor

Hot plate

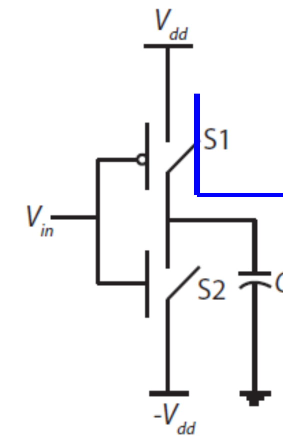
(<100 W/cm²)

4004, 8008, 8080, 8085, 8086, 80286, 80386, 80486, Pentium, Pentium Pro, Pentium II, III, IV, Itanium, Itanium 2, Core 2 Duo, i3, i5, i7

Power density (W/cm²): 10^{-1}, 10^{0}, 10^{1}, 10^{2}, 10^{3}, 10^{4}

Year: 1970, 1975, 1980, 1985, 1990, 1995, 2000, 2005, 2010, 2015

Basic CMOS Unit:



Power: $P \sim N(CV_{dd}^2 f + P_{off})$

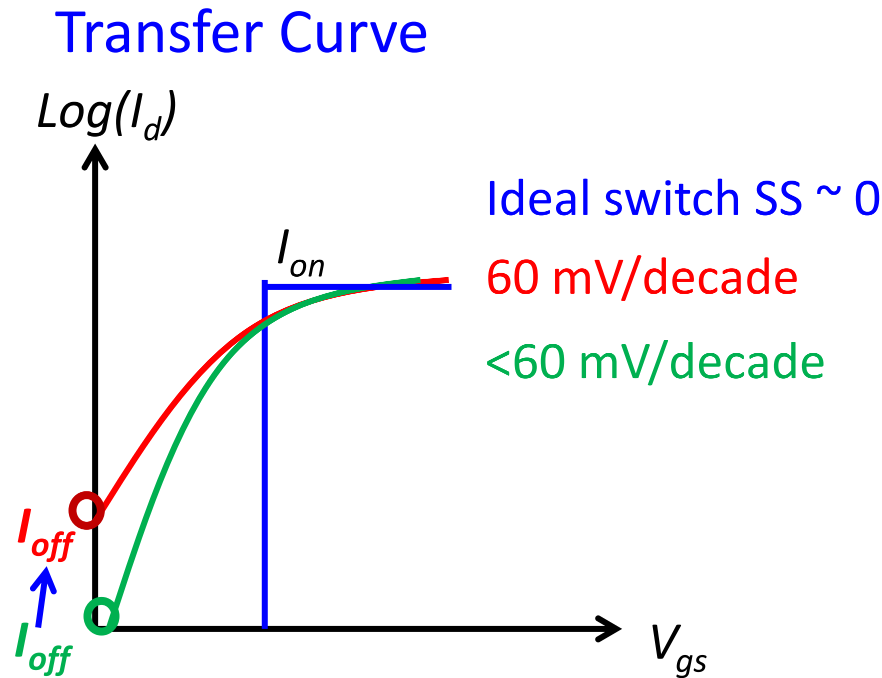
- Large Static and dynamic power dissipation in large scaled ICs
- Large amount of heat generated in ICs
- Limits the scaling and computing Performance of ICs

Ref.:1) G. L. Snider et. al., IEEE Nanotechnology, 2012 (for Intel data).
2) J. D. Meindl et. al., Science, 2001, vol. 293, pp. 2044

REQUIREMENT OF ENERGY-EFFICIENT DEVICES

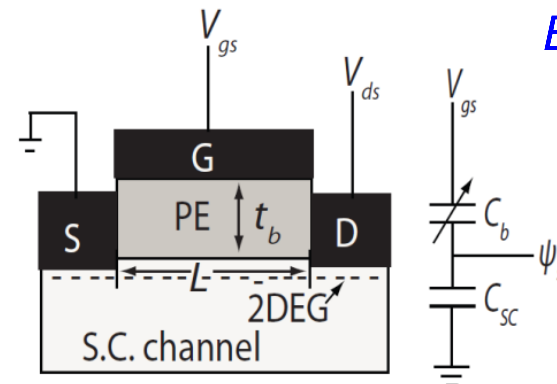
Possible Solution: Steep Slope FET switch → < 60 mV/decade steep switching in a FET

Transfer Curve



Allows further voltage V_{dd} Scaling in ICs & reduce power dissipation

FET schematic:



Band diagram

E(eV)

$f(E - E_F) \sim e^{-E/kT}$

V_{gs}

E_F

$f(E)$

V_{ds}

x

Subthreshold Slope:

$$SS = \frac{\partial V_{gs}}{\partial (log_{10} I_d)}, = \frac{\partial V_{gs}}{\partial \psi_s} \frac{\partial \psi_s}{\partial (log_{10} I_d)} = m \times 60 \text{ mV/dec}$$

Modify electrostatics → 'body factor'

Modify transport → TFETs/I-MOS

❖ Need to modify these factors for < 60 mV/decade!

Existing Ideas: 1) TFETs/I-MOS, 2) Negative capacitance using ferroelectric gate material (Internal voltage step up)

NEGATIVE CAPACITANCE IN FERROELECTRIC GATE INSULATOR

Subthreshold Slope:

$$SS = \frac{\partial V_{gs}}{\partial(log_{10} I_d)},$$

$$= \frac{\partial V_{gs}}{\partial \psi_s} \frac{\partial \psi_s}{\partial(log_{10} I_d)}$$

$$= \left(1 + \frac{c_s}{c_{ins}}\right) \times 60mV/dec$$

Internal voltage gain:

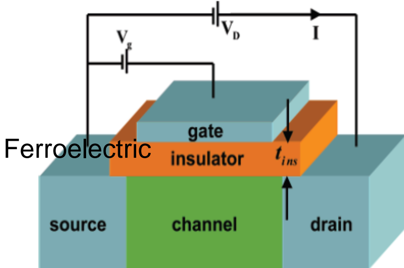
$$\frac{\partial \Psi_s}{\partial V_{gs}} > 1$$

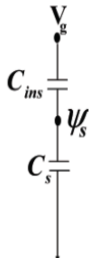
SS < 60 mV/decade

$C_{ins} < 0$

Negative curvature of energy

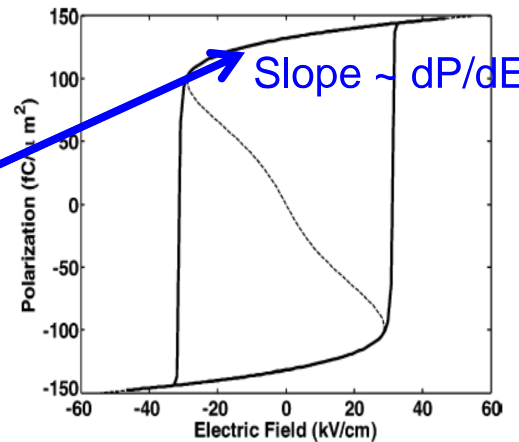
Negative capacitance at free energy maxima

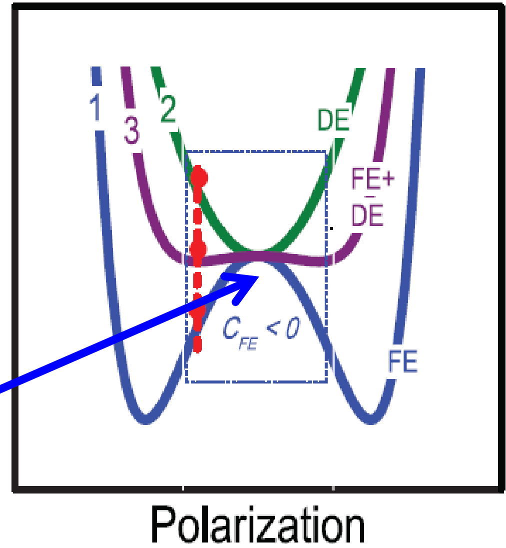




Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices

Sayeef Salahuddin* and Supriyo Datta†





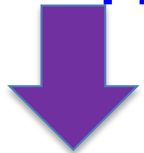
Ref. : 3. S. Salahuddin et. al. Nano. Lett., vol.8, 405, 2008
4. A. Khan et.al. Appl. Phys. Lett. 99, 113501 (2011)

ELECTROSTRICTION IN PIEZOELECTRIC GATE BARRIER

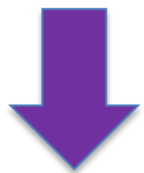
Mechanism:

Electrostriction

External Applied Voltage

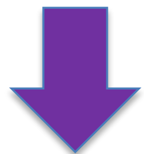


Piezoelectric Material (AlN)

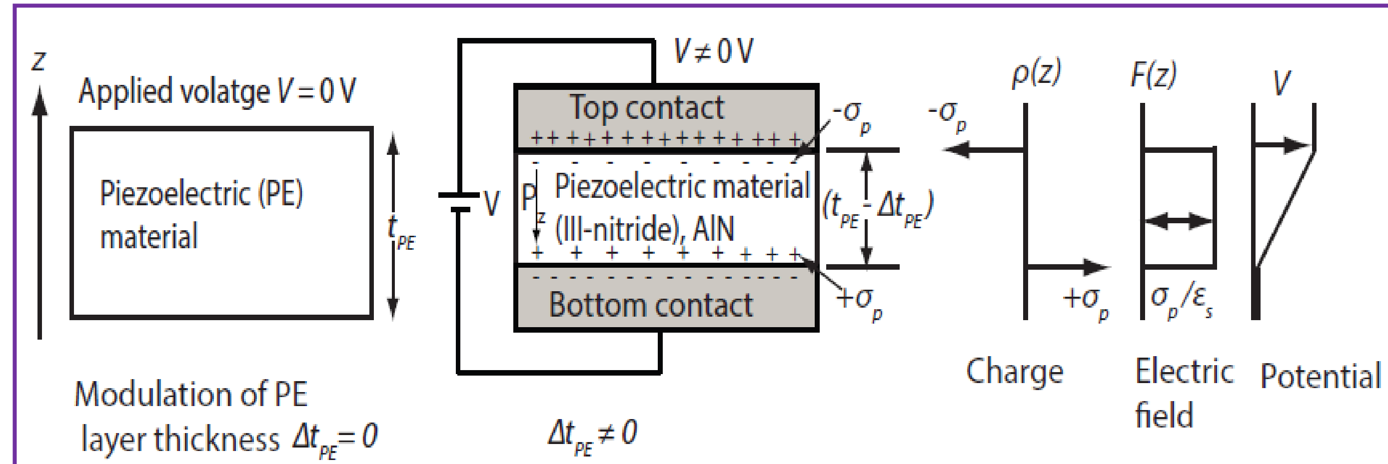


Electrostatic attractive force: σ_P^2/ϵ_{33}

Electric field-induced deformation of PE layer



Modulation of PE barrier thickness with applied bias: $(t_{PE} - \Delta t_{PE})$

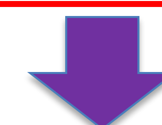


Voltage drop across the PE layer:

$$V = [(\sigma_P + \sigma_{sp} \mp e_{33} \cdot \gamma_{33})/\epsilon_{33}] \times (t_{PE} - \Delta t_{PE})$$

$$\Delta t_{PE}/t_{PE} = \sigma_P^2/C_{33}\epsilon_{33}$$

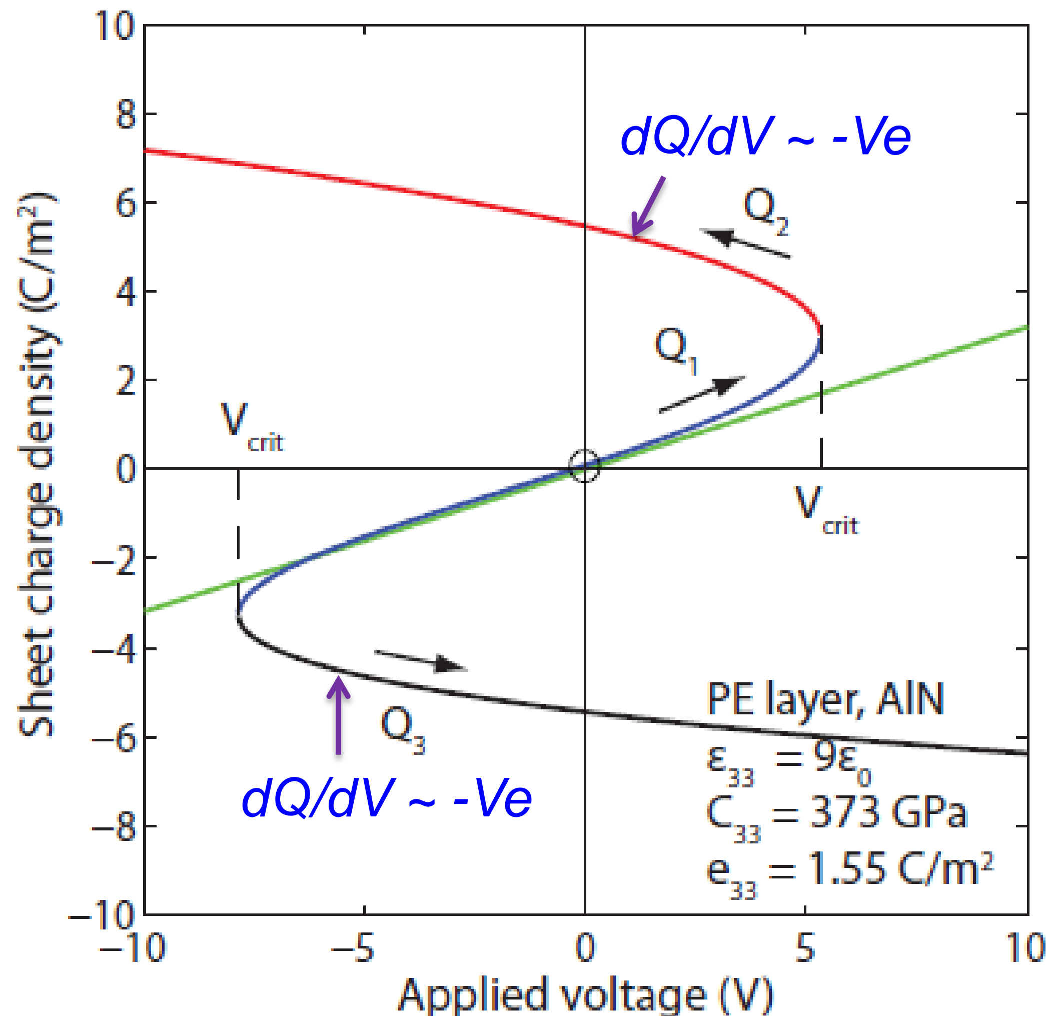
$$\pm\frac{e_{33}t_{PE}}{C_{33}^2\epsilon_{33}^3} \cdot \sigma_P^4 - \frac{t_{PE}}{C_{33}\epsilon_{33}^2} \cdot \sigma_P^3 + \left(\mp\frac{e_{33}t_{PE}}{C_{33}\epsilon_{33}^2} - \frac{t_{PE}}{C_{33}\epsilon_{33}^2} \cdot \sigma_{sp}\right) \cdot \sigma_P^2 + \frac{t_{PE}}{\epsilon_{33}} \cdot \sigma_P + \frac{t_{PE}}{\epsilon_{33}} \cdot \sigma_{sp} - V = 0.$$



4th order non-linear charge equation

CHARGE STATES IN THE PIEZOELECTRIC LAYER

Charge vs. Voltage Curve



Mechanism:

Electrostriction

Charge states (Q2 & Q3)
(Negative capacitance)

Charge state (Q1)
(Positive capacitance)

Normal Charge state
($Q = C_{geo} V$)

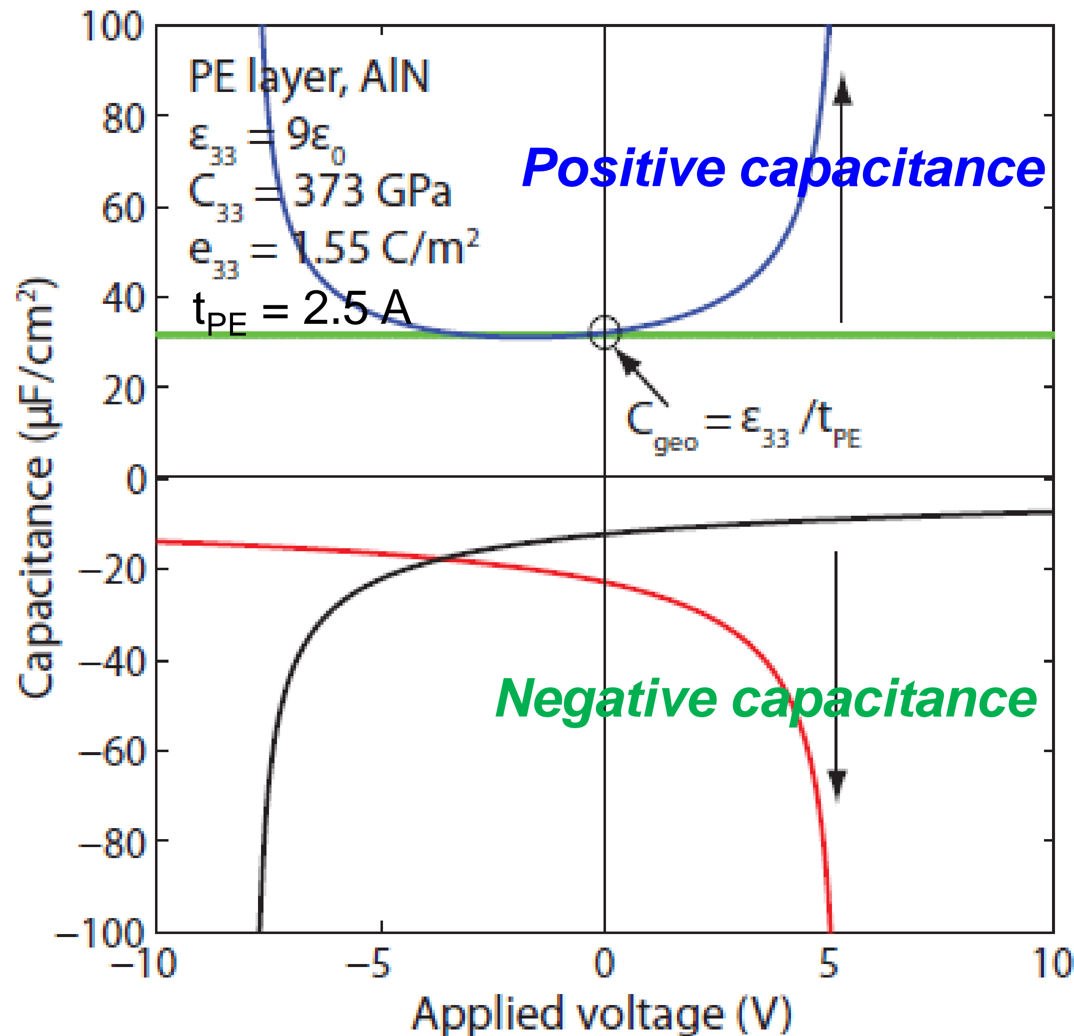
Constant geometric capacitance

Driving Force:

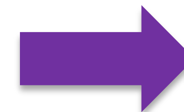
- ❖ **Large Field-Induced Deformation**
- ❖ **Strong Electromechanical Interaction**
- ❖ **Higher Piezoelectricity**
- ❖ **Higher Spontaneous Polarization**

ELECTROMECHANICAL CAPACITANCE

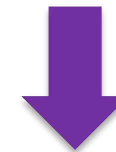
Capacitance vs. Voltage Curve



- Voltage-dependent capacitance for different charge states due to electrostriction in PE layer



Results in negative capacitance in the PE layer



Motivates to use as *active* gate barriers for Steep Slope FETs

FET structure with piezoelectric gate barrier

Change in free energy density in PE layer:

$$H = \frac{1}{2}C_{ijkl}\gamma_{ij}\gamma_{kl} - \frac{1}{2}\epsilon_{ij}E_iE_j - e_{ijk}E_i\gamma_{jk} - E_iP_i$$

$$\gamma_{zz} = -P_z^2/(C_{33}\epsilon_{33})$$

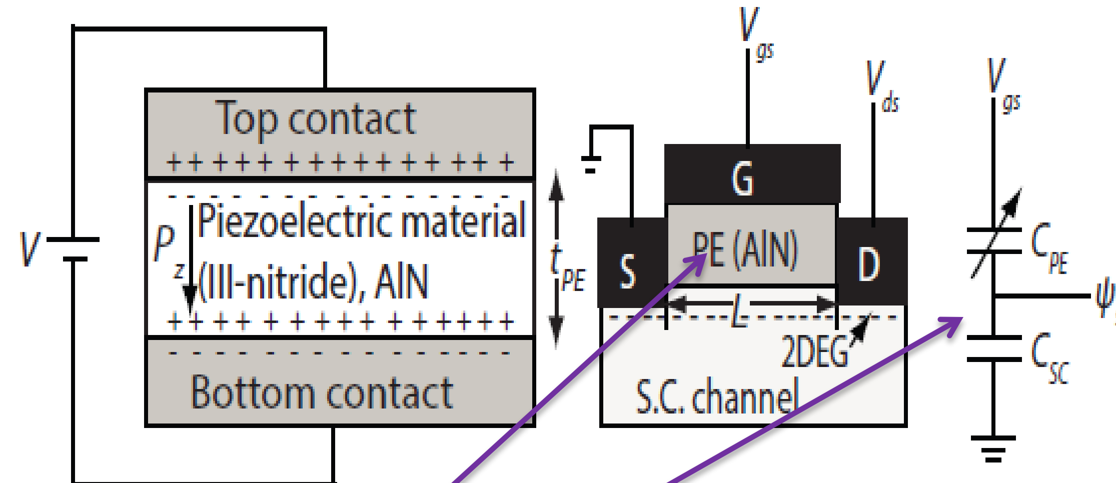
$$\left(\frac{2.t_{PE}}{C_{33}\varepsilon_{33}^2}\right)\cdot\sigma_P^3 + \left(\frac{3e_{33}t_{PE}}{C_{33}\varepsilon_{33}^2}\right)\cdot\sigma_P^2 - \left(\frac{t_{PE}}{\varepsilon_{33}}\right)\cdot\sigma_P - V = 0,$$

$$\sigma_P = C_{sc}\psi_s$$

$$\alpha_3\psi_s^3 + \alpha_2\psi_s^2 - \alpha_1\psi_s - (V_{gp} - \psi_s) = 0,$$

Surface Potential Eq.

Device Structure:



Piezoelectric material: *Active Gate barrier*

Coefficients:

$$\alpha_3 = \left(\frac{2t_{PE}}{C_{33}\epsilon_{33}^2}\right)\cdot C_{sc}^3,$$

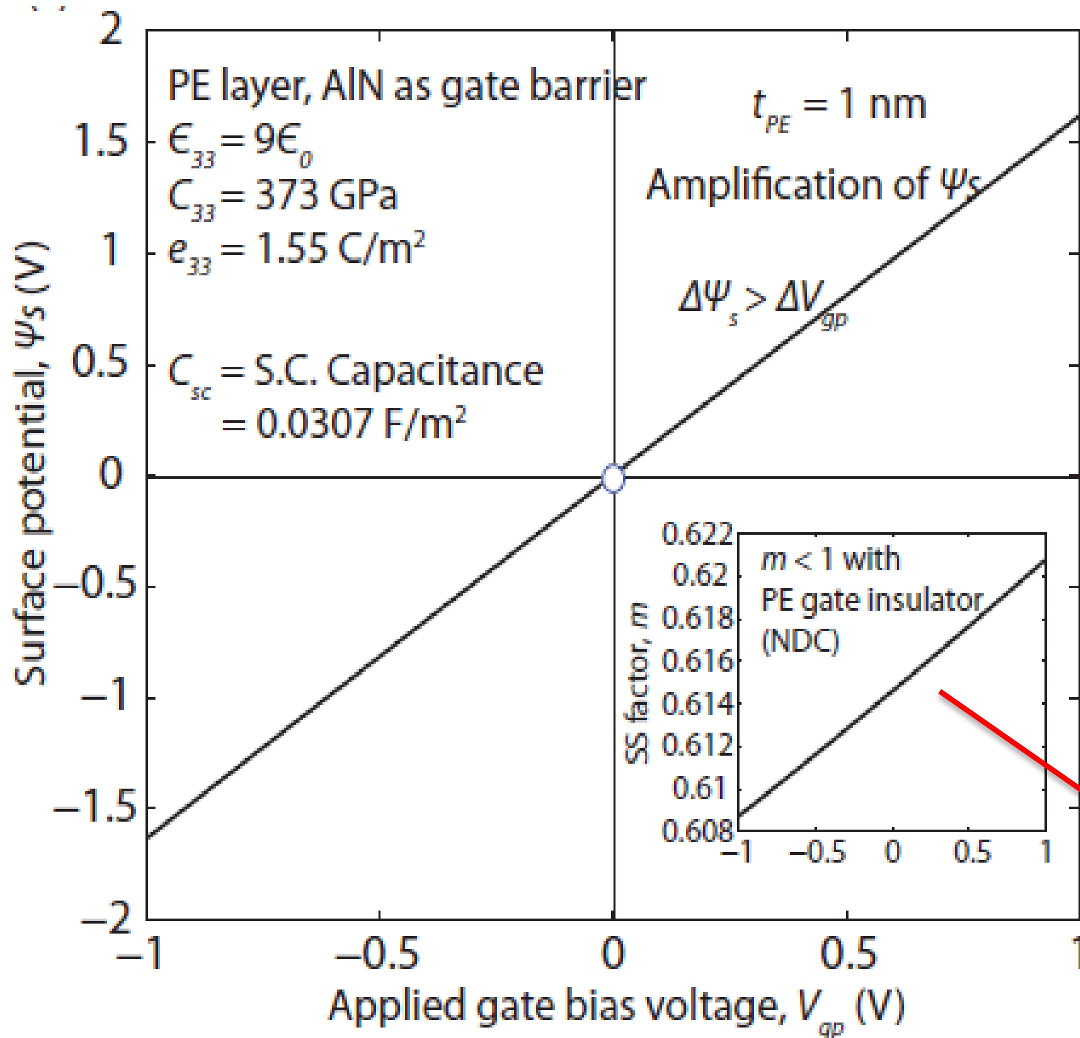
$$\alpha_2 = \left(\frac{3e_{33}t_{PE}}{C_{33}\epsilon_{33}^2}\right)\cdot C_{sc}^2,$$

$$\alpha_1 = \left(\frac{t_{PE}}{\epsilon_{33}}\right)\cdot C_{sc}.$$

Ref. 5: Jogai et. al., J. Appl. Phys., vol. 94, pp. 6566–6572, 2003.

SURFACE POTENTIAL & STEEP SS

Surface Potential vs. Gate Bias Voltage



Amplification of Surface Potential Relative to Gate Voltage

Subthreshold Slope (SS):

$$SS = \frac{\partial V_{gs}}{\partial(log_{10} I_d)}, = \frac{\partial V_{gs}}{\partial \psi_s} \frac{\partial \psi_s}{\partial(log_{10} I_d)}$$

$m < 1$

Body factor

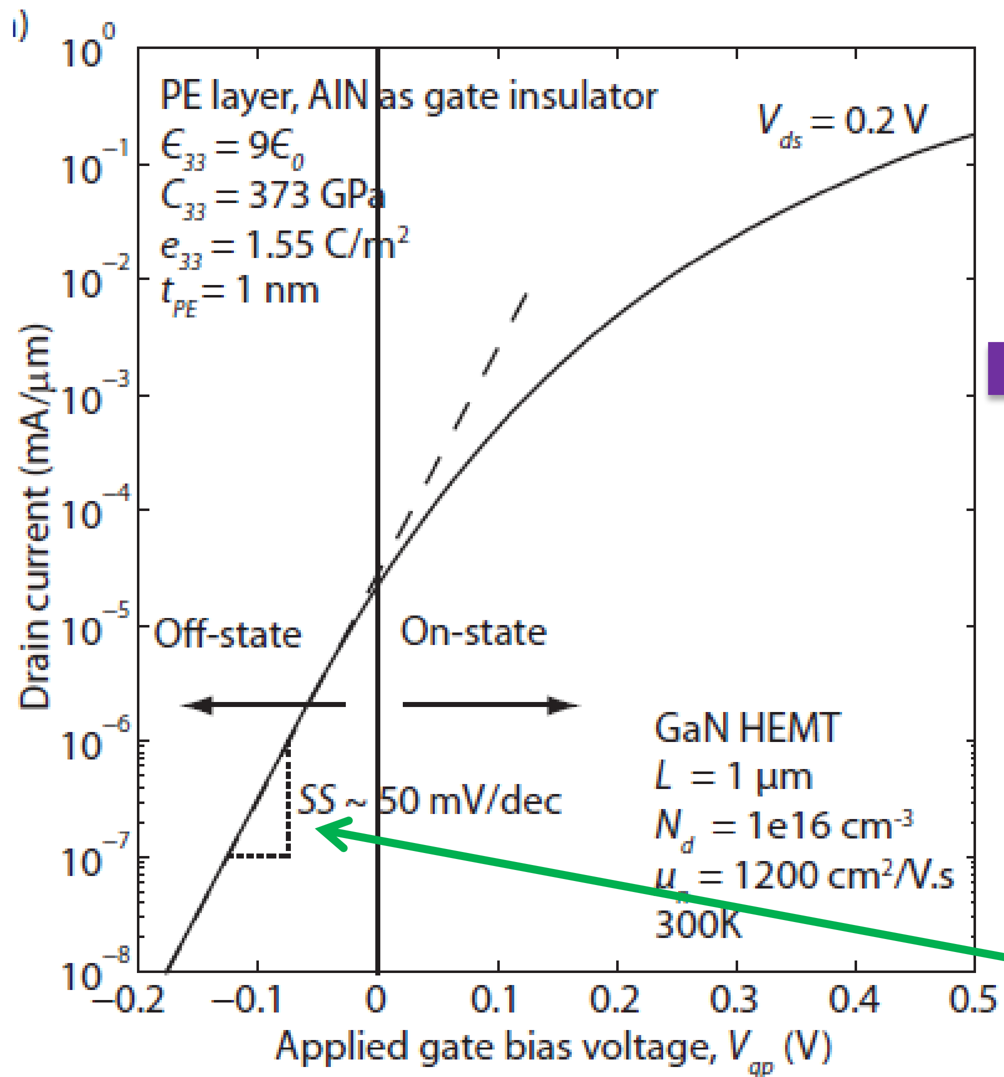
$$SS = m \times 60 \text{ mV/dec}$$

$m < 1$

SS < 60 mV/dec

TRANSISTOR CHARACTERISTICS & STEEP SS

Transfer Curve

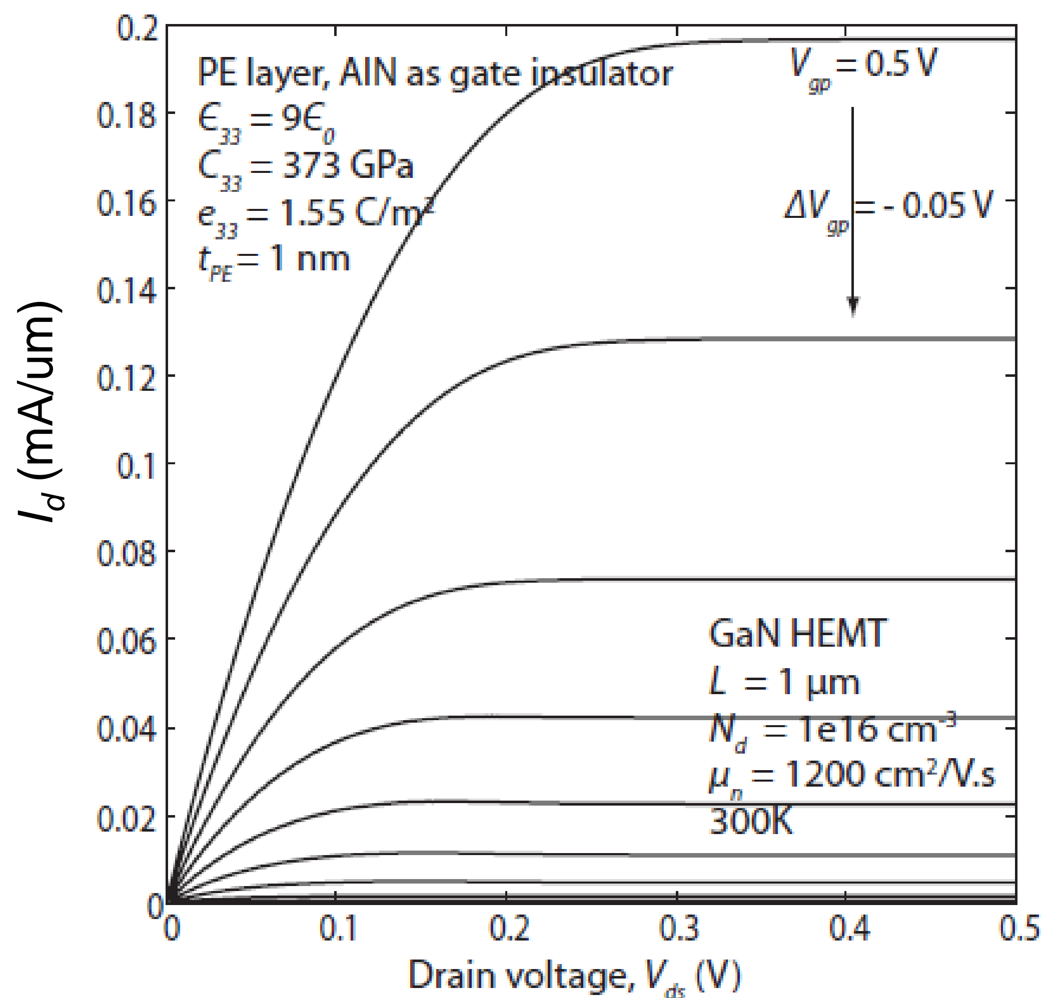


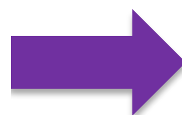
- Use of PE (AlN) gate barrier with NDC
- GaN channel HEMT
- Use of ψ_s-based Compact model
- Steep Subthreshold Slope ~ 50 mV/decade

R. Jana et. al., DRC, 2012

OUTPUT CHARACTERISTICS

I-V characteristics:





- Use of PE (AlN) gate barrier with NDC
- GaN channel HEMT
- Use of ψ_s-based Compact model

CONCLUSION

- We showed NDC in a thin piezoelectric layer (t_{PE} < 5 nm) using electric field-induced electrostriction effect in the layer
- Proposed piezoelectric material as the *active* gate barrier for energy-efficient steep slope transistors
- Electrostriction & piezoelectricity internally amplify the channel surface potential over the applied gate bias voltage
- Showed internal voltage gain and *sub-60 mV/decade* subthreshold switching using Polar piezoelectric barrier
- Model for an AlN barrier in the GaN channel HEMT predicts *50 mV/decade* subthreshold slope

Acknowledgement

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Thank You for your Attention!