Device Design Considerations for Ultra-Thin Body Non-Hysteretic Negative Capacitance FETs

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Outline

• Introduction
• Background of Negative Capacitance FET (NCFET)
• Design considerations
• Simulation of UTB NCFET
• Conclusion
Vdd scaling is slowing down

<table>
<thead>
<tr>
<th>Node (nm)</th>
<th>250</th>
<th>180</th>
<th>130</th>
<th>90</th>
<th>65</th>
<th>32</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd (V)</td>
<td>2.5</td>
<td>1.8</td>
<td>1.3</td>
<td>1.2</td>
<td>1.1</td>
<td>0.9</td>
<td>0.8</td>
</tr>
</tbody>
</table>

IC Vdd scaling history and ITRS projection

Boltzmann statistics lead to 60mV/decade limit.

Source: C. Hu, IEDM 2010
# Sub-60mV/dec Swing FETs

<table>
<thead>
<tr>
<th>Tunnel FET</th>
<th><strong>STRUCTURE</strong></th>
<th><strong>SWITCHING MECHANISM</strong></th>
</tr>
</thead>
</table>
| **Feedback FET** | ![Tunnel FET Diagram](image) | **Band-To-Band Tunneling**  
- Reverse-biased P-I-N |
| **A Padilla, *IEDM 2008*** | | |

| **Negative Capacitance FET** | ![Negative Capacitance FET Diagram](image) | **Internal Feedback**  
- Forward-biased P-I-N |
| **S. Salahuddin, *Nano lett. 2008*** | | |

| **Negative Capacitance Amplification** | | |

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**SWITCHING MECHANISM**

- **Band-To-Band Tunneling**
  - Reverse-biased P-I-N

- **Internal Feedback**
  - Forward-biased P-I-N

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**Negative Capacitance Amplification**
The Negative Capacitor

Landau Theory of Ferroelectric

Khan et al. APL 99, (2011)
Capacitance Model for Negative Capacitance FET

Schematic of NCFET

Capacitance Model of NCFET

- \( V_G \)
- \( V_MOS \)
- \( C_{FE} \)
- \( C_{ox} \)
- \( C_{dep} \)
- \( C_{MOS} \)

Underlying MOSFET
Capacitive Divider

\[ V_{MOS} = V_G \]

\[ V_{MOS} = V_G \frac{C_{FE}}{C_{FE} + C_{MOS}} \]

Since \( C_{FE} \) can be negative:

\[ V_{MOS} = V_G \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \]

Condition 1:
For large amplification, \(|C_{FE}| \) should be close to \( C_{MOS} \)
Use Negative Capacitance to Reduce the Subthreshold Swing

**Schematic of Negative Capacitance FET**

**Underlying MOSFET**

**Formula:**

$$SS \ of \ NCFET = 60 \text{mV/dec} \ast \left(1 + \frac{C_{dep}}{C_{ox}}\right) \ast \frac{1}{A_V}$$
Subthreshold Swing of NCFET

\[
SS \ of \ NCFET = 60mV/\text{dec} \times \left(1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} - \frac{C_{\text{dep}}}{|C_{FE}|}\right)
\]

Condition 2:
For swing < 60mV/dec
\[\Rightarrow |C_{FE}| < Cox\]
(sets the maximum value for |C_{FE}|)

\[
C_{ox}' = \frac{C_{ox}^*|C_{FE}|}{|C_{FE}| - C_{ox}}
\]
Condition for no hysteresis

\[
SS \text{ of NCFET} = 60mV/\text{dec} \times \left(1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} - \frac{C_{\text{dep}}}{|C_{FE}|}\right)
\]

For stable operation (no hysteresis):
\[
\left(\frac{C_{\text{dep}}}{C_{\text{ox}}} - \frac{C_{\text{dep}}}{|C_{FE}|}\right) \text{ must be larger than } -1
\]

\[
\Rightarrow \left(\frac{C_{\text{dep}}}{C_{\text{ox}}} - \frac{C_{\text{dep}}}{|C_{FE}|}\right) > -1
\]

\[
\Rightarrow \frac{1}{|C_{FE}|} < \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{dep}}}
\]

\[
\Rightarrow |C_{FE}| > C_{\text{MOS}}
\]

Condition 3:
For no hysteresis, \(|C_{FE}|\) must be larger than \(C_{\text{MOS}}\)
(set the minimum value for \(|C_{FE}|\))

\[
A_v = \frac{|C_{FE}|}{|C_{FE}| - C_{\text{MOS}}}
\]
The “window” of $C_{FE}$

**Condition 1:**
For small swing, $C_{FE}$ should be $\sim C_{MOS}$

**Condition 2:**
If swing < 60mV/dec
$\Rightarrow |C_{FE}| < Cox$

**Condition 3:**
For no hysteresis, $|C_{FE}|$ must be larger than $C_{MOS}$
Choosing the $|C_{FE}|$ value

![Graph showing the capacitance $(C_{MOS})$ vs. gate voltage $(V_G)$ with $|C_{FE}|$ indicated.]
The Capacitance Mismatch

\[ A_v = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \]
What do we need?

We need a underlying MOSFET with a larger depletion capacitance.
Device Optimization: 
UTB with Extremely Thin BOX

By using a thin body and a thin BOX, $C_{dep}$ can be increased.
Simulation of Negative Capacitance FET Structure

Coupled 2D Electrostatics-1D Landau Simulation

Ferroelectric: 1-D Landau Simulation. PbZr$_{0.5}$Ti$_{0.5}$O$_3$. Anisotropy Constants from Haun et al., Ferroelectrics 99, 63 (1989)

Intrinsic MOSFET (2D): TCAD Sentaurus Simulation.

Interlayer Metallic Electrode: To screen out non-uniformity in potential profile as well due to domain formation.
Effect of varying $T_S$

Effect of varying $T_S$ on the $I_{DS}$ ($\mu A/\mu m$) vs $V_{GS}$ (V) characteristics for different $T_S$ values. The figure illustrates the impact of varying gate-source overlap capacitance $C_{ox}$ and substrate oxide capacitance $C_{BOX}$ on device performance.
Simulated Id-Vg of UTB NCFET

$\text{Lg}=32\text{nm}, \ \text{Ts}=0.7\text{nm}, \ \text{Tox}=3\text{nm}, \ \text{Tbox}=1\text{nm}$
Summary

The graph shows the relationship between the supply voltage $V_{DD}$ (mV) and the average subthreshold swing (mV/dec) as well as the ON current density ($I_{ON}$ (µA/µm)) for different gate lengths ($L_g$), oxide thicknesses ($t_{ox}$), and BOX thicknesses ($t_{box}$). The parameters used are:

- $L_g = 32$ nm
- $t_s = 0.7$ nm
- $t_{box} = 1$ nm
- $t_{ox} = 3$ nm

The graph indicates a linear increase in Avg. SS with $V_{DD}$ and a non-linear increase in $I_{ON}$ with $V_{DD}$. The configuration with $L_g = 32$ nm shows the highest Avg. SS and $I_{ON}$ compared to other configurations.
Conclusion

• NCFET can operate hysteresis free.
• For sub-60mV/dec and no hysteresis, there is a maximum and minimum constraint for $C_{FE}$.
• UTB design can reduce the issue of capacitance mismatch.
• Simulation shows NCFET can achieve swing of sub-30mV/dec from pA/μm to μA/μm with estimated $I_{ON}$ of 0.250mA/μm at 0.3V $V_{DD}$.
Acknowledgements

This work was partially supported by Office of Naval Research, the FCRP MSD center, Qualcomm, and NSF E3S Center at Berkeley.
• Thank you!
\[
\frac{\partial \varphi_s}{\partial V_G} = \frac{\partial \varphi_s}{\partial V_{MOS}} * \frac{\partial V_{MOS}}{\partial V_G} = \frac{C_{ox}}{C_{ox} + C_{dep}} * \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}}
\]
\[
\frac{\partial \varphi_s}{\partial V_G} = \frac{C_{ox}}{C_{ox} + C_{dep}} * \frac{|C_{FE}|}{|C_{FE}| - \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}}}
\]
\[
SS = \frac{\partial V_G}{\partial V_{MOS}} * \frac{\partial V_{MOS}}{\partial \varphi_s} * \frac{60mV}{dec}
\]
\[
= \frac{60mV}{dec} * \left( 1 + \frac{C_{dep}}{C_{ox}} - \frac{C_{dep}}{|C_{FE}|} \right)
\]
• $E_c \sim 30k \text{ to } 300k\text{V/cm}$
• $\sim 0.003 \text{ to } 0.03\text{V/nm}$
Material Exploration for Ferroelectric Negative Capacitance

Three Different Ferroelectric Negative Capacitance Model Systems has been identified so far.

1. \( \text{Pb(Zr}_{0.2}\text{Ti}_{0.8})\text{O}_3, > 225 \, ^\circ\text{C} \)
2. \( \text{PbTiO}_3, > 110 \, ^\circ\text{C} \)
3. \( (\text{Ba}_{0.8}\text{Sr}_{0.2})\text{TiO}_3 > 110 \, ^\circ\text{C} \)

Negative Capacitance in sub-10nm Films:
\( \text{Ba}_{0.8}\text{Sr}_{0.2}\text{TiO}_3-\text{LaAlO}_3 \) superlattice

With three different negative capacitance material system identified, the stage is set for making the first crystalline NCFET.
MOSFET Scaling: The Negative Capacitance Approach

**Moore’s Law**

![Graph showing subthreshold leakage increasing with technology scaling](image)

**Negative Capacitance FET**

![Diagram of a negative capacitance FET](image)

Salahuddin et al., Nanoletters 8, 405 (2008).

Negative capacitance can give $S < 60 \text{ mV/decade}$

Fabrication of Negative Capacitance FET for simultaneous High Performance-Ultra Low Power Operation for Mobile Computing
Landau-Devonshire Theory of Ferroelectrics tells that Ferroelectric capacitors can give rise to negative capacitance under certain conditions.
Epitaxial Growth of Nanoscale Ferroelectric Heterostructure

<table>
<thead>
<tr>
<th>Material</th>
<th>Type</th>
<th>a-axis parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pb(Zr_{0.2}Ti_{0.8})O_{3}</td>
<td>Ferroelec</td>
<td>3.953 A</td>
</tr>
<tr>
<td>SrTiO_{3}</td>
<td>Dielectric</td>
<td>3.905 A</td>
</tr>
<tr>
<td>SrRuO_{3}</td>
<td>Metal</td>
<td>3.92 A</td>
</tr>
</tbody>
</table>

Excellent Epitaxial Quality, Interface Roughness 2-3 unit cells

TEM Courtesy: Prof. X. Pan, UMich
Material Exploration for Ferroelectric Negative Capacitance

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2. PbTiO₃, > 110 °C
3. (Ba₀.₈Sr₀.₂)TiO₃ > 110 °C

Negative Capacitance in sub-10nm films: Ba₀.₈Sr₀.₂TiO₃-LaAlO₃ superlattice

With three different negative capacitance material system identified, the stage is set for making the first crystalline NCFET.
Ultrafast polarization switching in thin-film ferroelectrics

J. Li, B. Nagaraj, H. Liang, W. Cao, Chi. H. Lee, and R. Ramesh

Materials Research Science and Engineering Center, University of Maryland, College Park, Maryland 20742

(Received 3 July 2003; accepted 3 December 2003)

We present an experimental approach to study the ultrafast polarization switching dynamics in thin-film ferroelectrics. A semiconductor photoconductive switch with femtosecond laser illumination is used as a “pulse generator” to produce jitter-free, sub-100 ps rise time step-function-like electrical pulses. Quantitative measurements yield a polarization switching time, $t_s$, of $\sim 220$ ps when measured with a 5 V, 68 ps rise time input electrical pulse. Modeling of the switching transients using the Merz–Ishibashi model and Merz–Shur model of switching kinetics yields a quantitative estimate of the characteristic switching time constant, $t_0$, of $\sim 70–90$ ps.

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