Full-quantum simulation of heterojunction TFET inverters providing better performance than Multi-Gate CMOS at sub-0.35V V_{DD}

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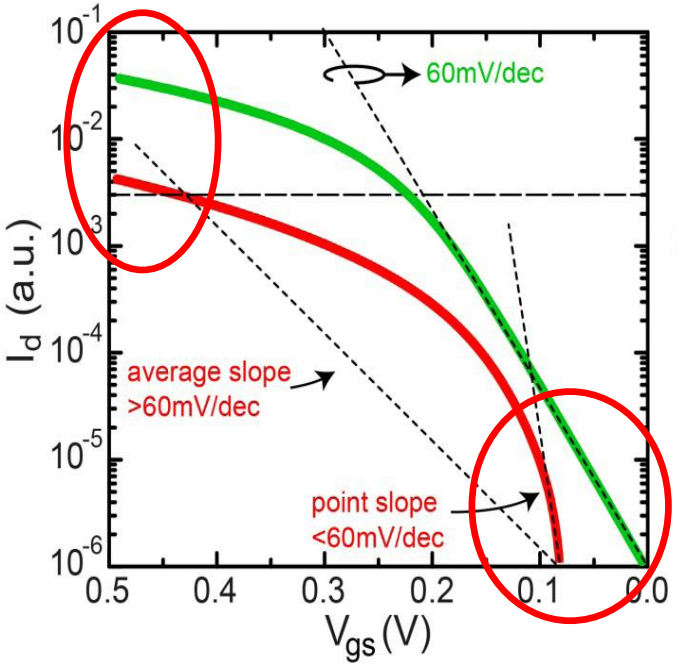
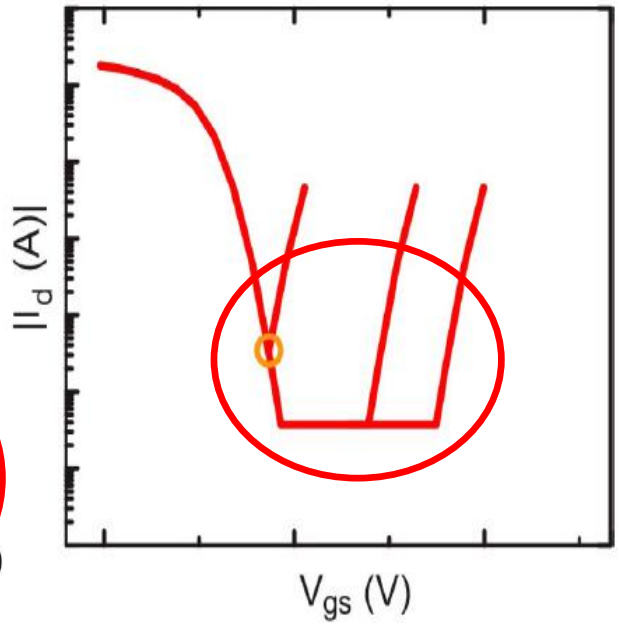
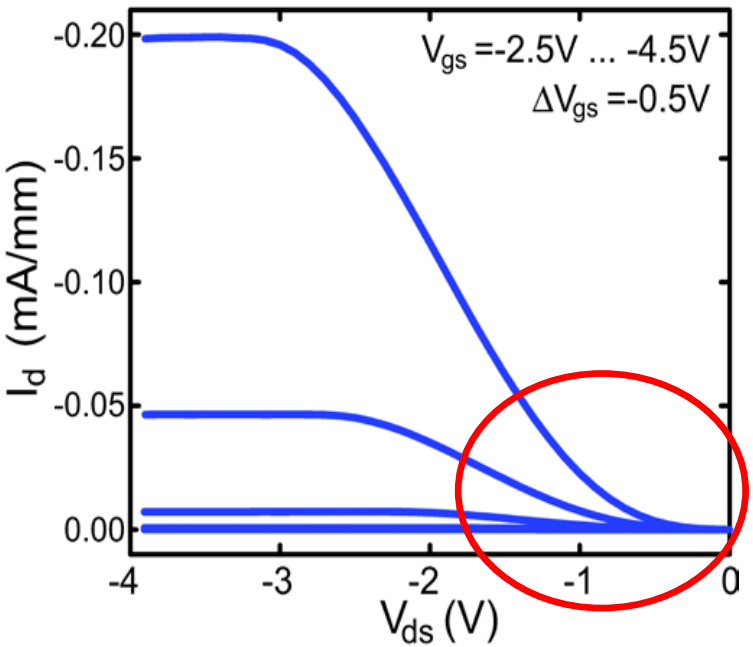
Outline

- Challenges of TFET design
- Optimization of complementary hetero-junction TFETs on the same technology platform
- TFET-based inverter design and speed-performance assessment
- Comparison with CMOS logic
- Conclusions

Challenges of TFET design







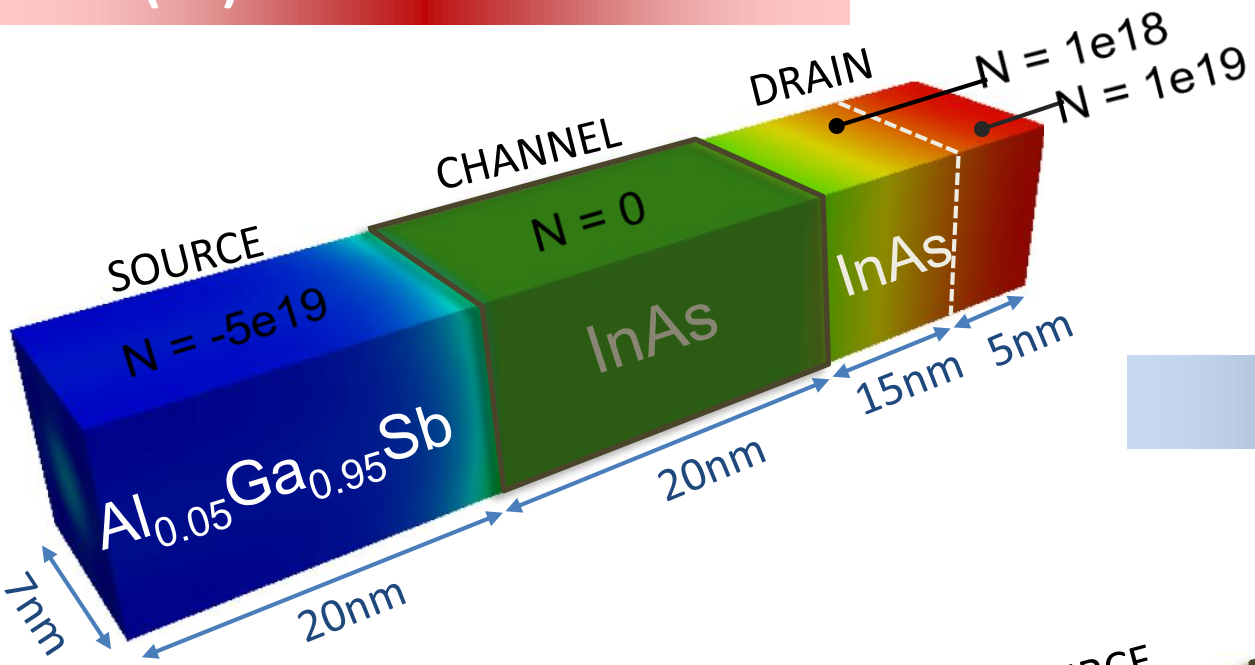
Simultaneously co-integrating n- and p-type devices on the same technology platform.

Design approach

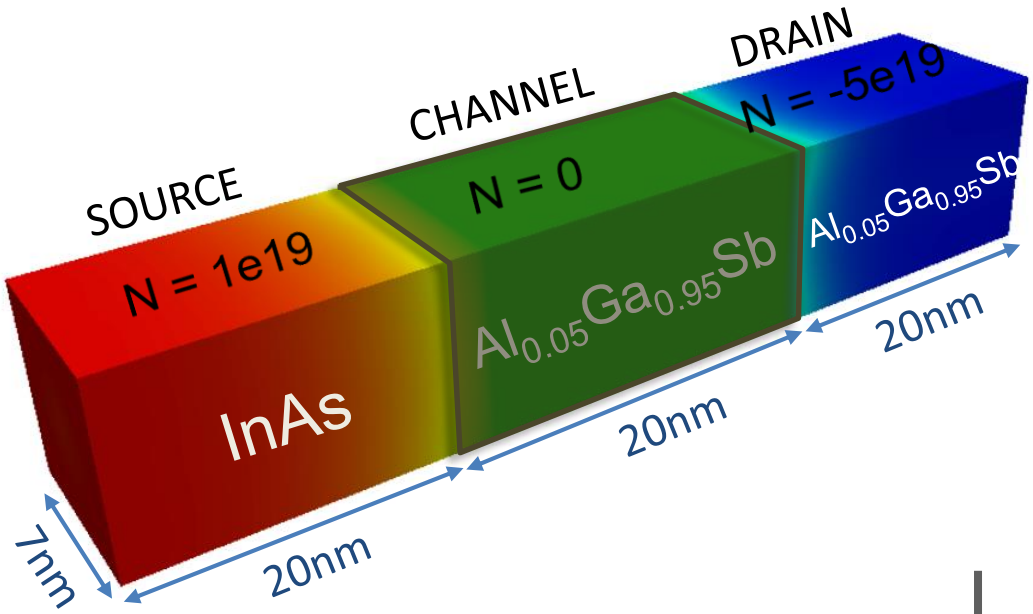
- The transmission probability is enhanced by an abrupt InAs-$Al_{0.05}Ga_{0.95}Sb$ heterojunction.
- Subthreshold slope and drain conductance are optimized by a suitable choice of the degeneracy level in the source and drain.
- Ambipolarity is controlled by drain engineering.
- The gate length is set at 20 nm in order to prevent direct source-to-drain tunneling; the cross section is thus 7x7 nm wide.
- Device optimization is carried out with a 3D full-quantum ***k·p*** simulation code.

Candidate devices

(Tn) 7nm-side n-TFET

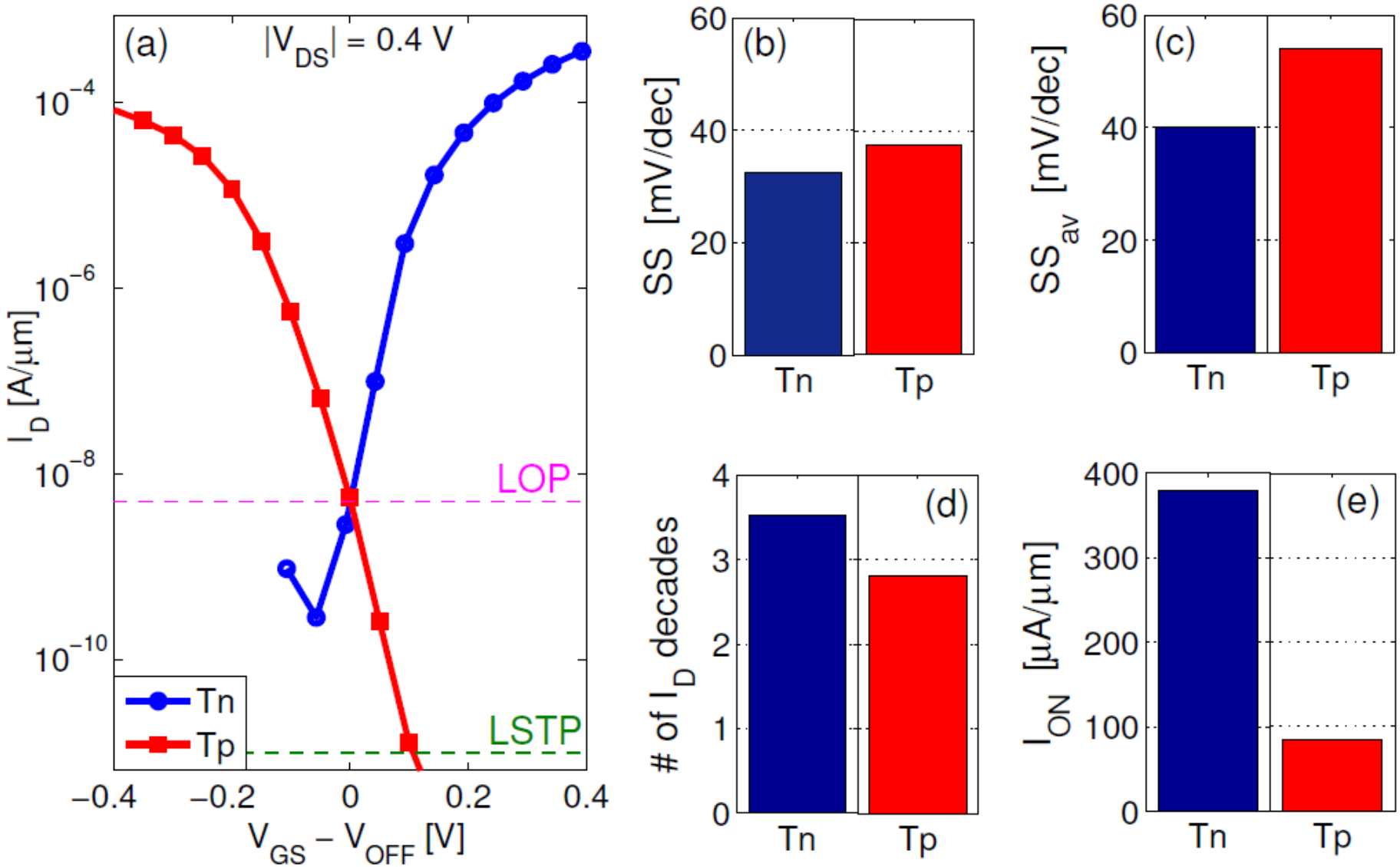


(Tp) 7nm-side p-TFET

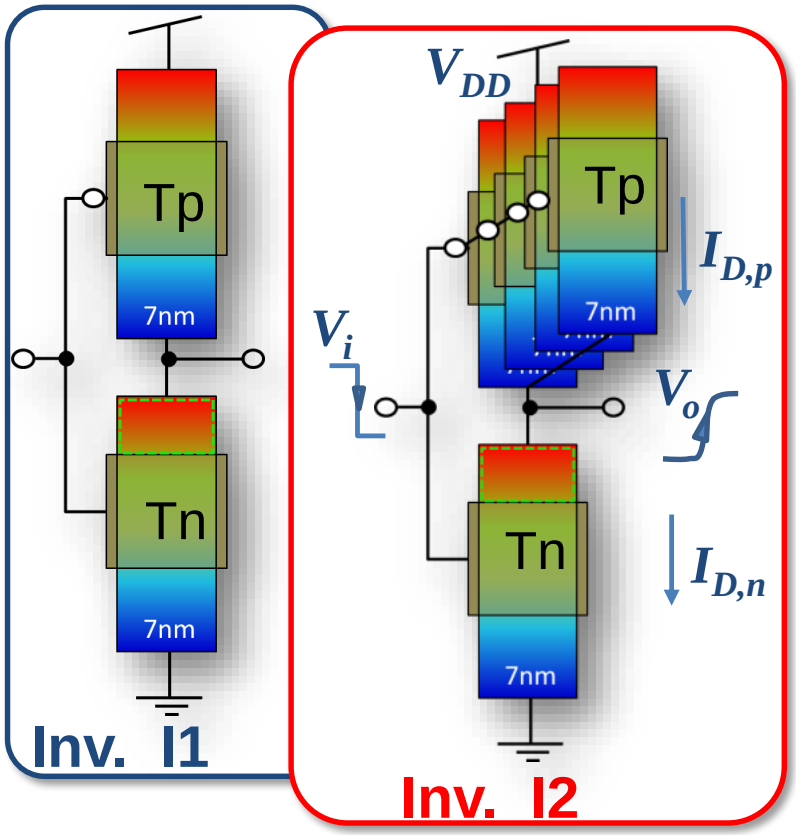


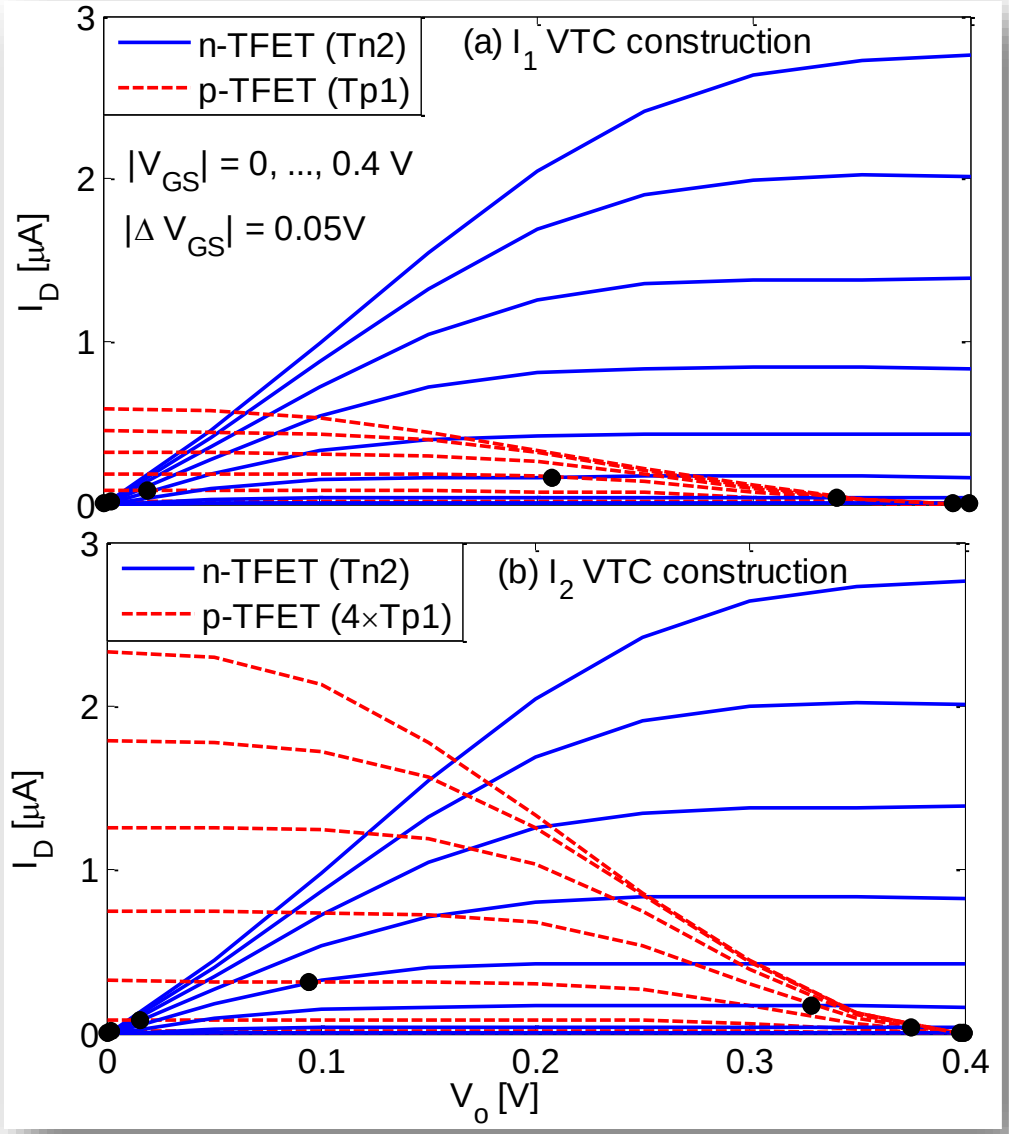
Al_2O_3 with EOT=1nm

Device performance @ V_{DD}=0.4 V



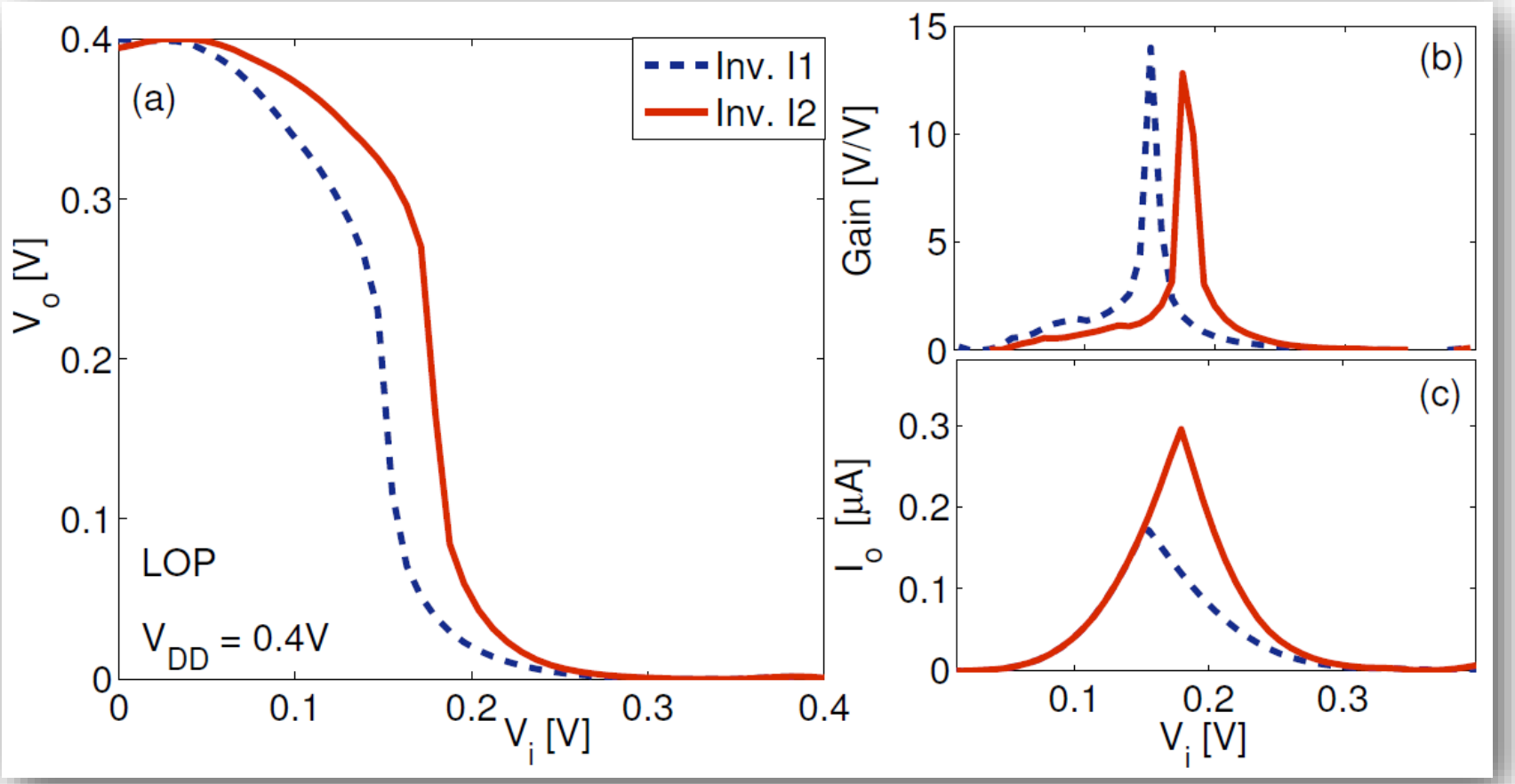
Inverter configurations





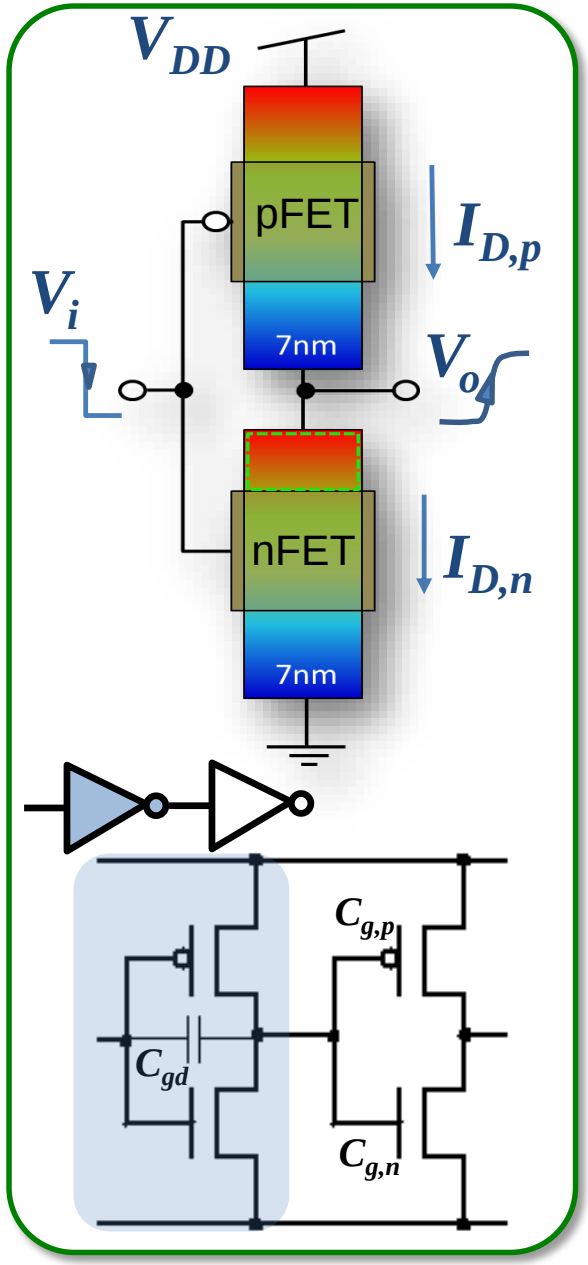
Inverter VTCs are constructed by combining I_D-V_{DS} families obtained by simulation in 0.05 V_{GS} steps and non-linear Interpolation

Static performance



- I1 has asymmetric VTC due to strong I_{ON} unbalance between Tn2 and Tp1
- This is compensated for in I2 by using 4xTp1
- In I2, WFs of the 4 Tp1 devices are adjusted to have $4xI_{OFF,\,p}=I_{OFF,\,n}=I_{OFF,\,LOP}$

Transient performance estimation



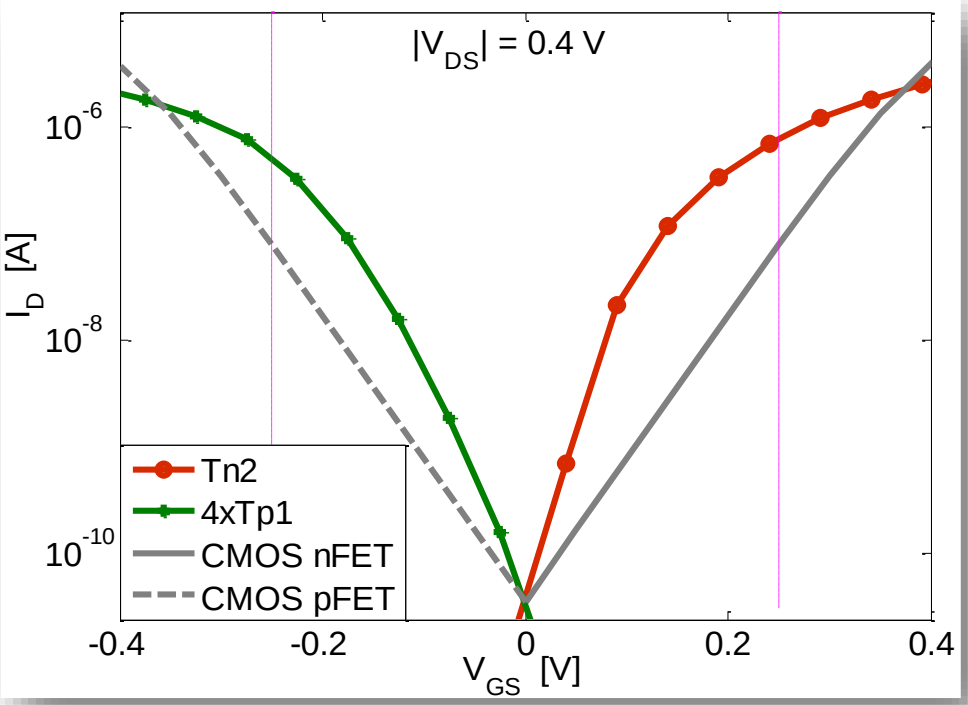
$$C_g = \frac{Q_{ON} - Q_{OFF}}{V_{DD}} \quad , \quad Q = q\int_{\Omega}(p - n + N)d\Omega$$

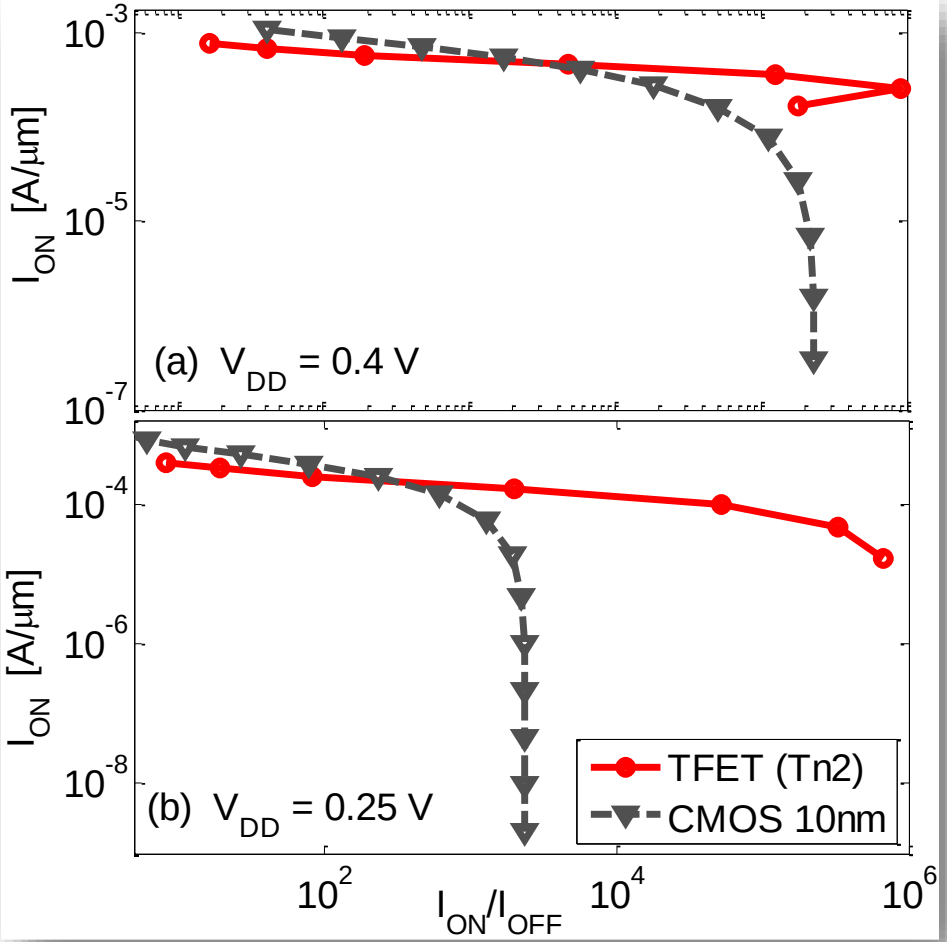
$$t_{r,f} = C_L \int_{0.1V_{DD}}^{0.9V_{DD}} \frac{dV_o}{|I_{D,p}(V_o) - I_{D,n}(V_o)|}$$

- **Device gate capacitance C_g is estimated from the integrated charge of the whole device in the off (Q_{OFF}) and on state (Q_{ON})**
- **10% to 90% rise/fall times $t_{r,f}$ are computed by integrating the drain currents at $V_{GS} = 0$ V or $V_{GS} = |V_{DD}|$ (assuming instantaneous input transitions)**
- **Miller effect expected to be significant for TFETs is accounted for as $C_M = 2 \times C_{gd}$, with $C_{gd} \approx 0.8 \times C_g$**

  $\rightarrow C_{load} = 2.6 \times (C_{g,n} + C_{g,p})$ for a self-loaded inv.

TFET-based I2 vs. CMOS



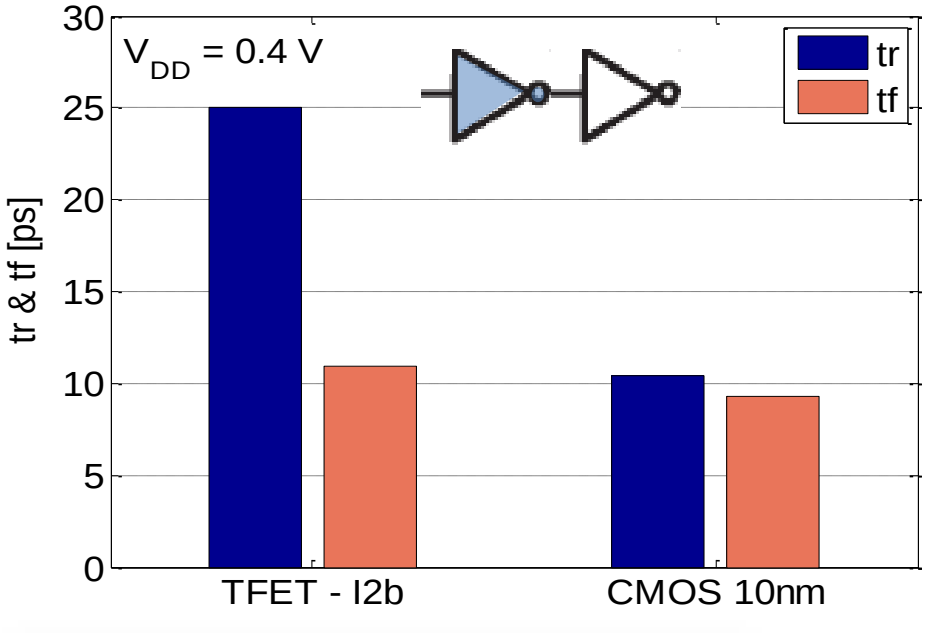


Node	L_{GATE}	W_{FIN}	H_{FIN}
10nm	14nm	9nm	21nm

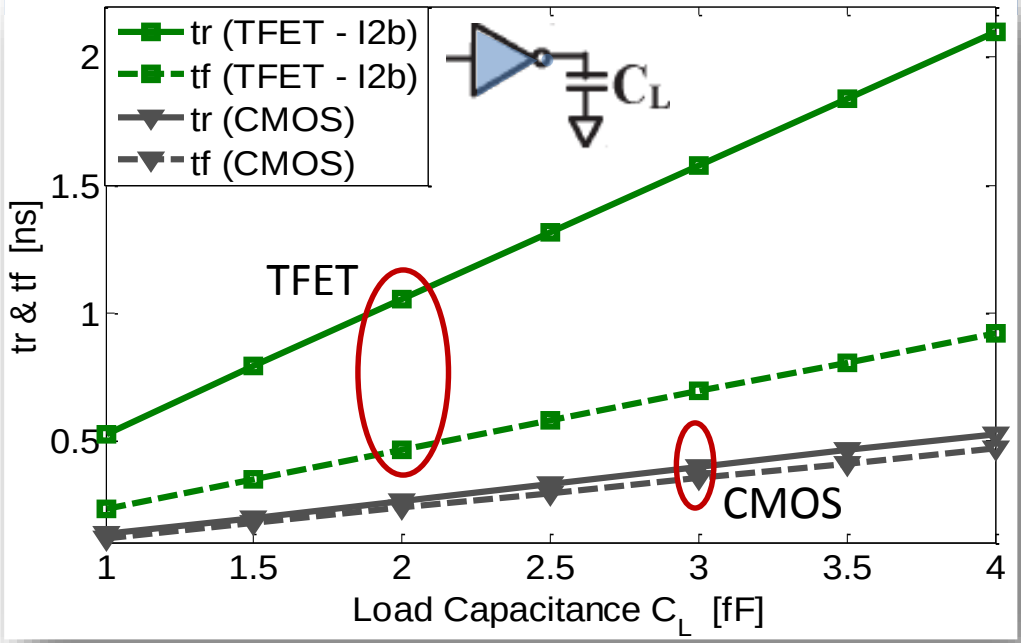
- **CMOS: 10nm FinFETs simulated using PTM-MG models in Spice**
- **WFs adjusted to make I_{OFF} (and static power) of FinFETs equal to that of TFETs**
- **TFET shows advantage at low V_{DD} (< 0.35 V)**

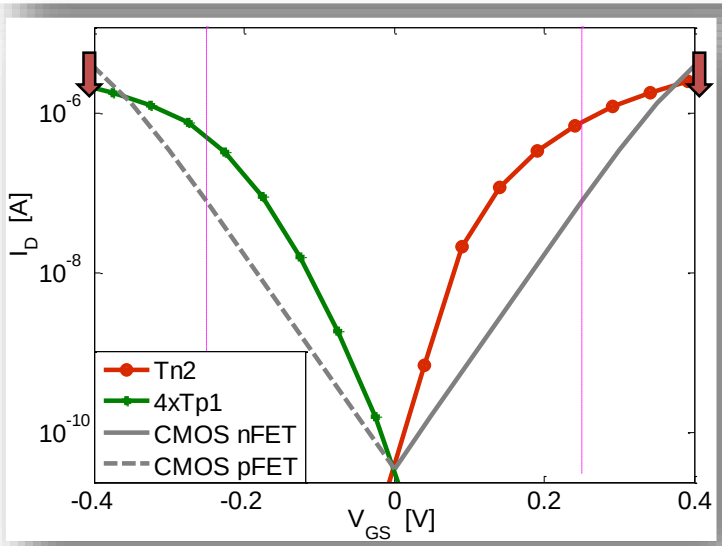
Comparison with CMOS @ V_{DD} = 0.4 V

Rise/fall times under self-loading



Rise/fall times under constant loading

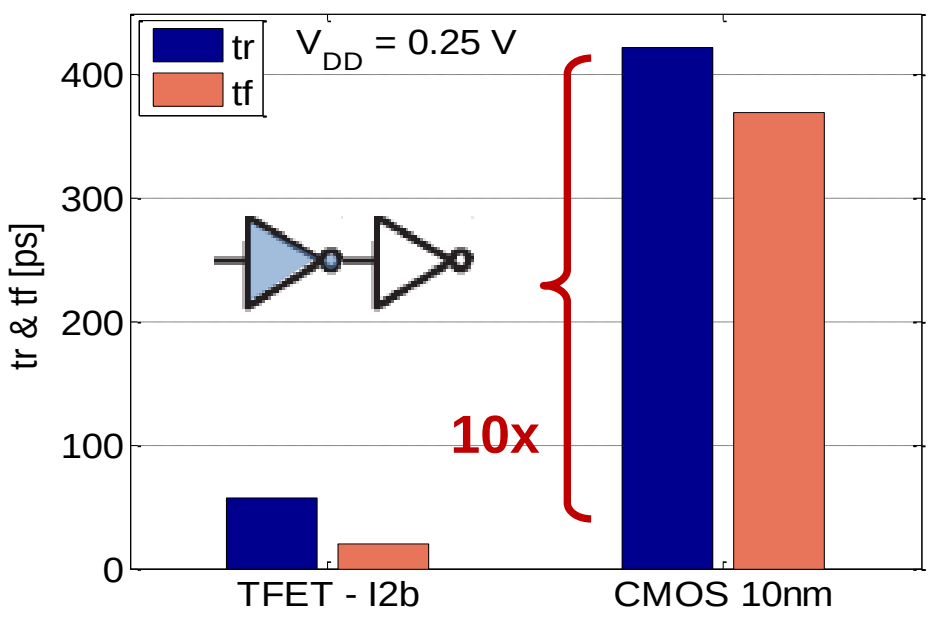




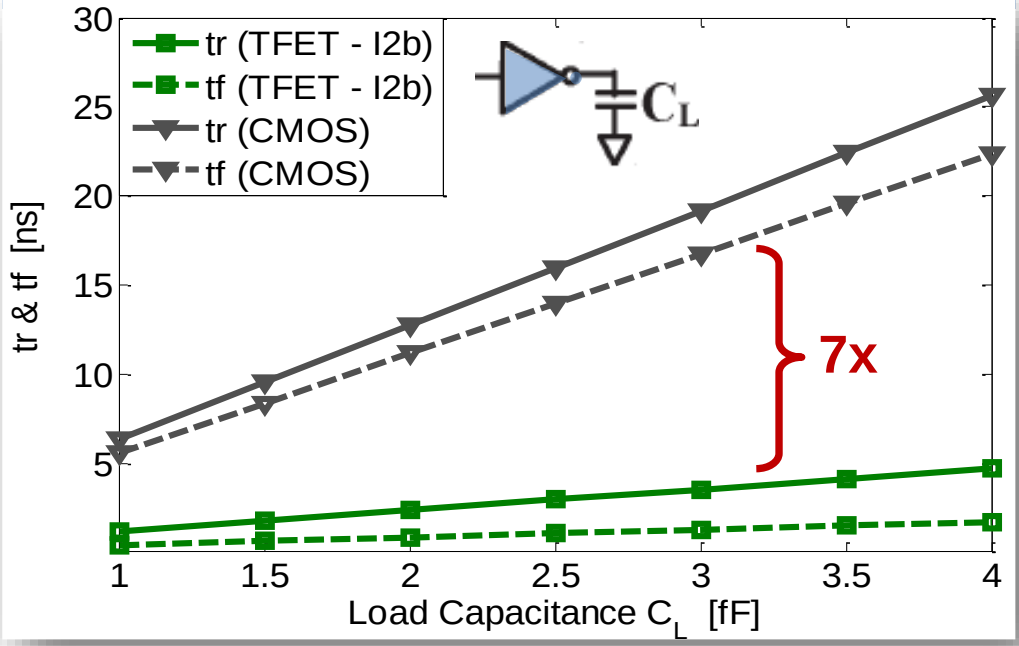
- **Miller effect and lower drive current make TFET inverter slower than CMOS under self-loading**
- **Under constant loading, Miller capacitance is negligible, but CMOS is faster due to higher drive current at V_{DD} = 0.4V**

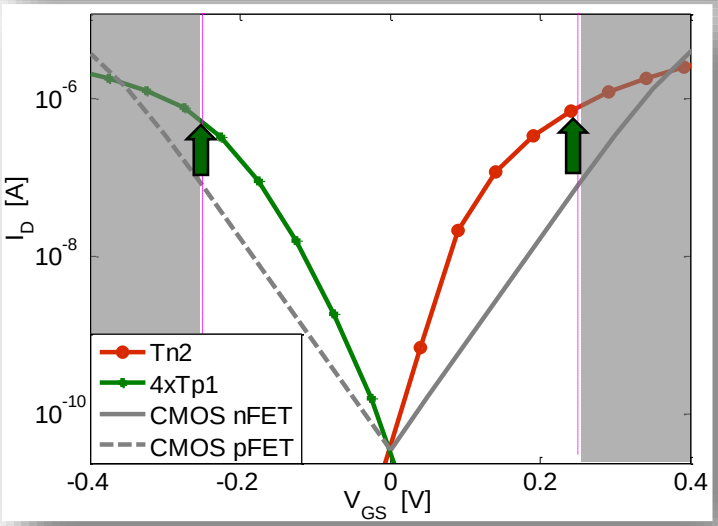
Comparison with CMOS @ V_{DD} = 0.25 V

Rise/fall times under self-loading



Rise/fall times under constant loading





- At V_{DD} = 0.25V, **TFET is substantially faster than CMOS** in both self-loading and constant-loading
- This is **due to the drive current advantage (≈10x)** associated with a steeper SS

Summary

- Optimized n- and p-type hetero-junction TFETs based on the $InAs/Al_{0.05}Ga_{0.95}Sb$ material pair have been designed
- The p-type TFET design requires substantial improvements in both I_{ON} current and drain conductance at low V_{DD}
- Comparison of TFET and CMOS inverter performance at the 10nm technology node:

  ↳ CMOS wins at V_{DD} = 0.4 V *BUT* TFET largely wins at V_{DD} = 0.25 V
- The analysis did not consider: *(i)* strain to improve TFET performance, *(ii)* carrier scattering, *(iii)* interface states.

  ↳ the obtained results should be regarded as qualitative indicators
- The rise/fall times at these limiting V_{DD} values are expected to be of the order of 10 ps or a few tens of ps for a self-loaded inverter

TFETs will find possible uses for low-power, moderate-performance applications