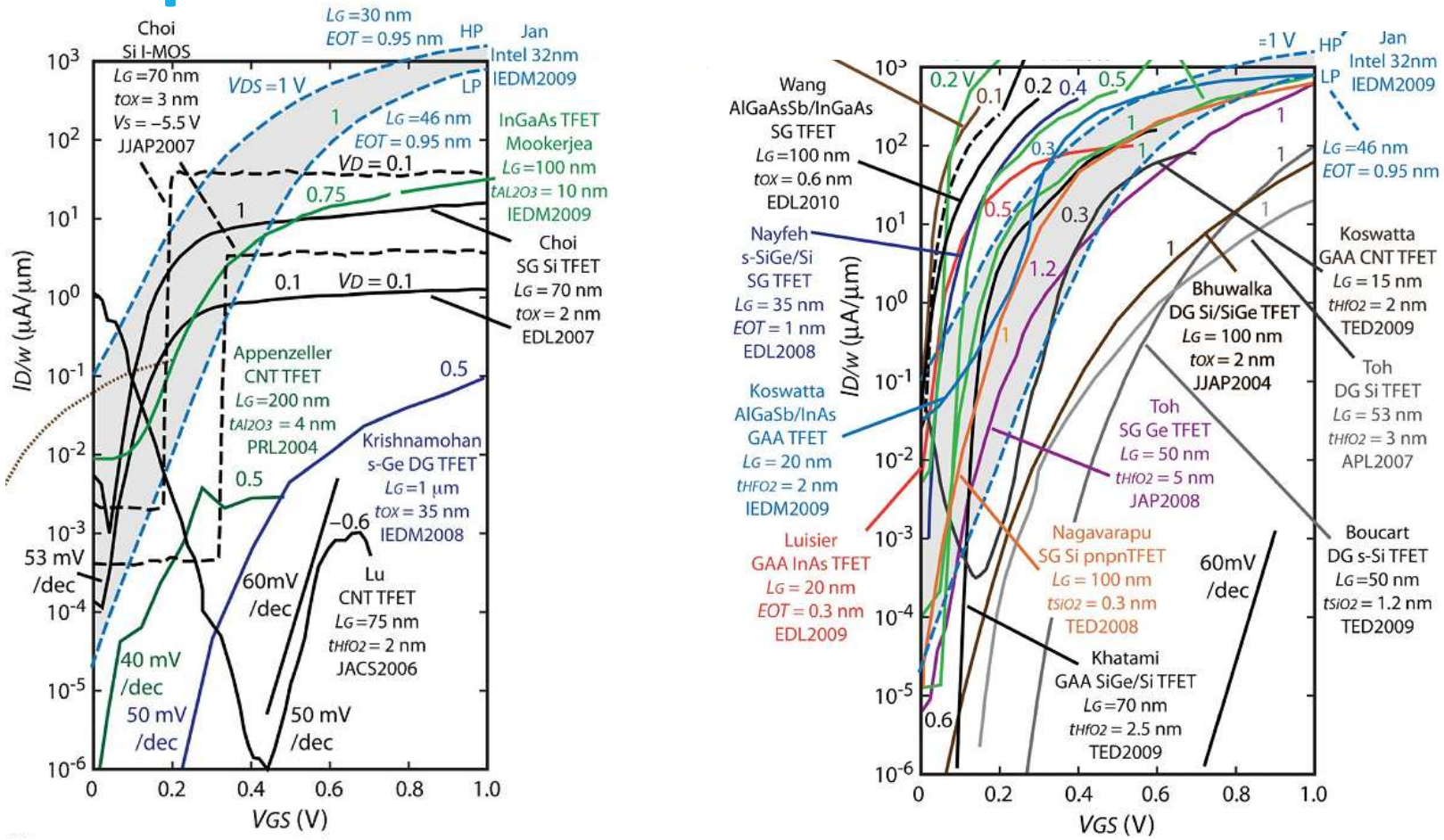
Electrostatic Design of Vertical Tunneling Field-Effect Transistors

James Teherani, Tao Yu
Profs. Dimitri Antoniadis, Judy Hoyt

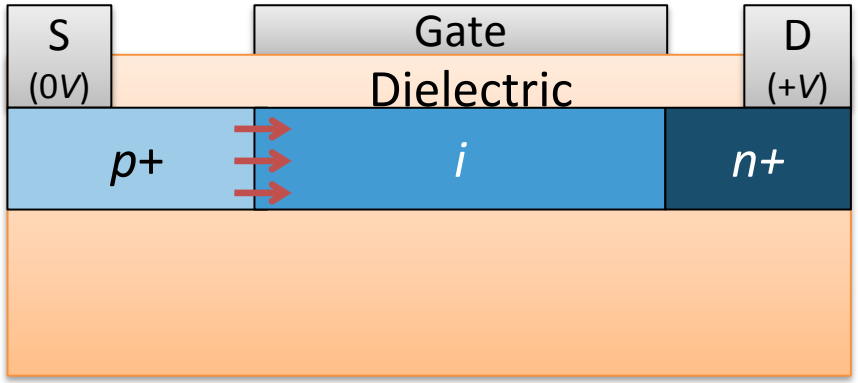
Third Berkeley Symposium on Energy Efficient Electronic Systems
October 29th, 2013

Discrepancy between TFET **Experiments** and **Simulations**



Seabaugh and Zhang, TED 2010.

Lateral and Vertical Structures



Lateral TFET

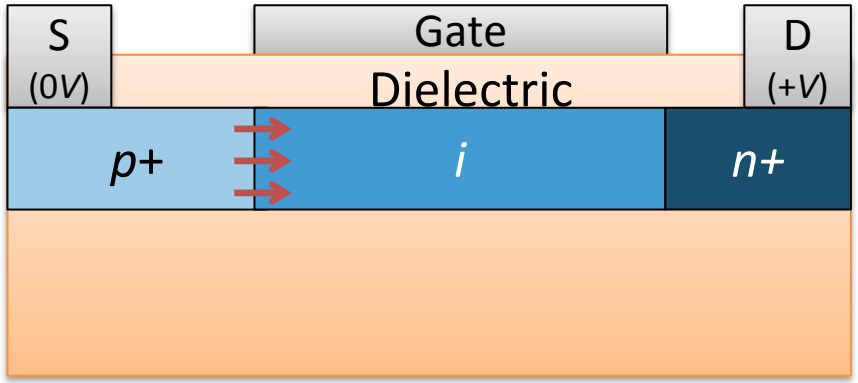
Advantages

- Scalable gate length ($I \not\propto L_G$)
- Simple design
  - Can be implemented in vertical nanowire

Disadvantages

- Tunneling only at gate edge
  - Gate alignment and S doping profile is critical!
- Direct S to D tunneling as $L_G \rightarrow 0$

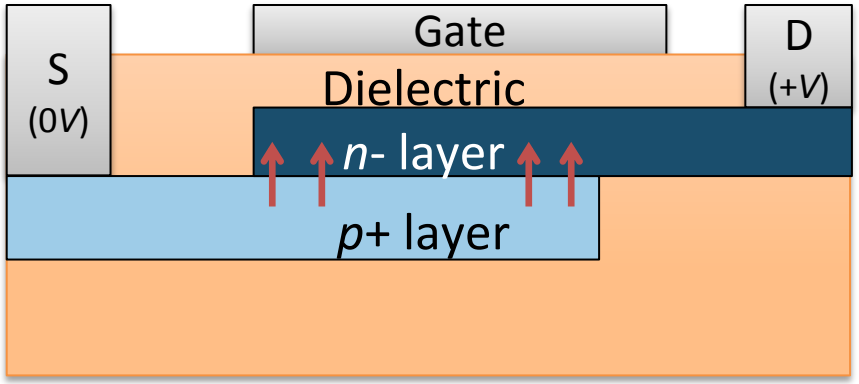
Lateral and Vertical Structures



Lateral TFET

Advantages
- Scalable gate length ($I \not\propto L_G$)
- Simple design
  - Can be implemented in vertical nanowire

Disadvantages
- Tunneling only at gate edge
  - Gate alignment and S doping profile is critical!
- Direct S to D tunneling as $L_G \rightarrow 0$

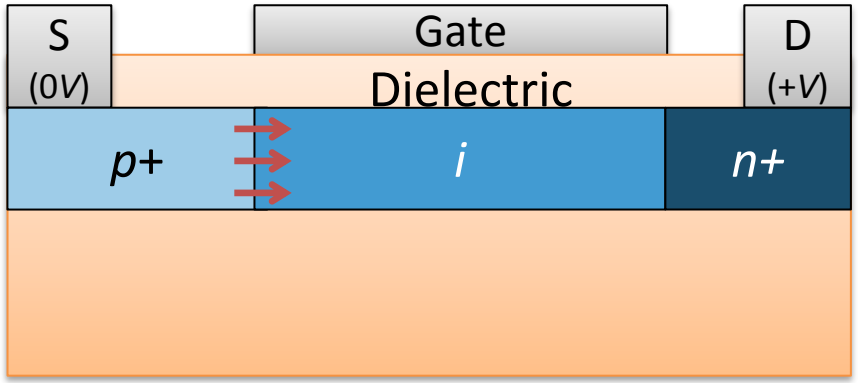


Vertical TFET

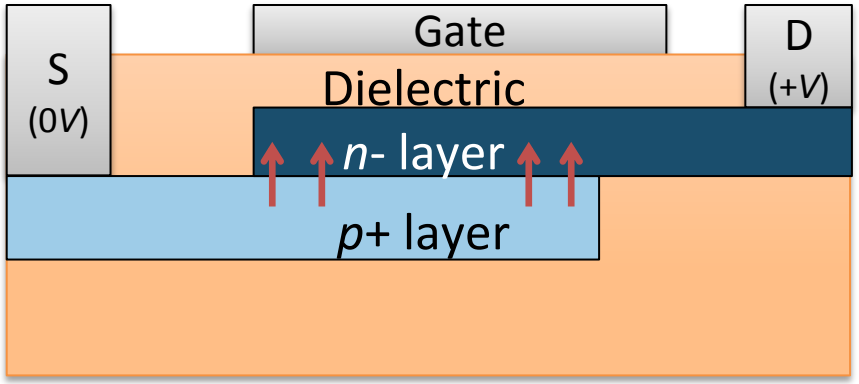
Advantages
- Enhanced gate control of tunneling area
  - Favorable electrostatics
- Tunneling under entire gate area
- Eliminates direct S to D tunneling

Disadvantages
- Current↓ as gate length ↓
- Difficult fabrication

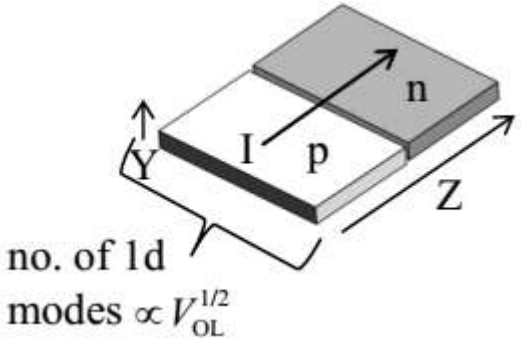
Dimensionality Analysis

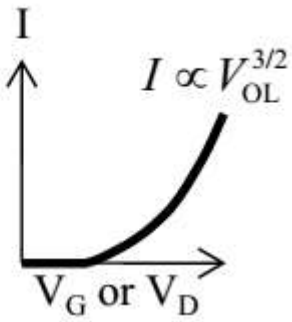


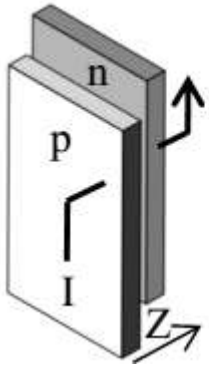
Lateral TFET

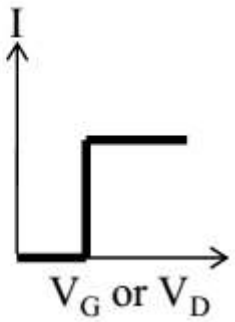


Vertical TFET



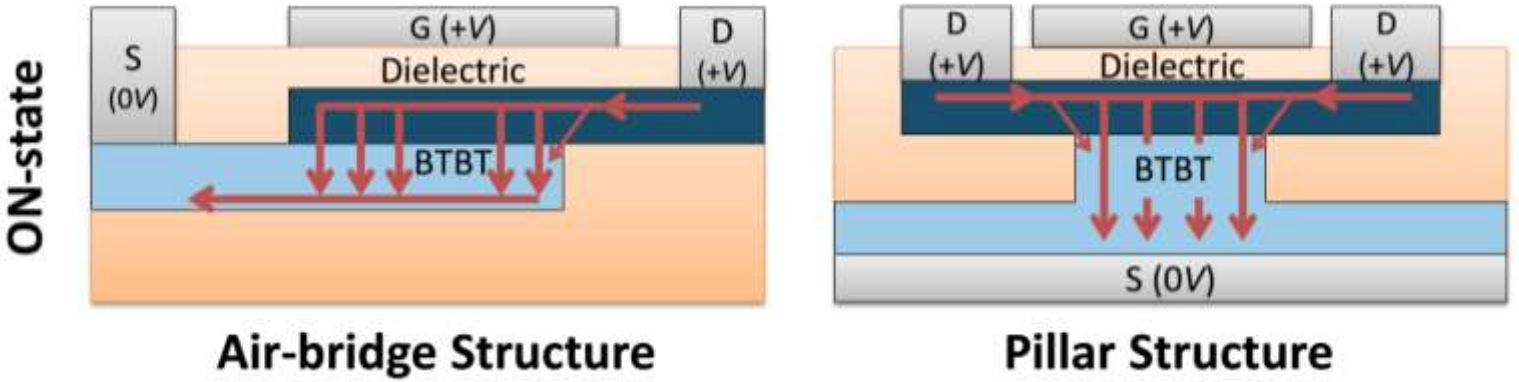




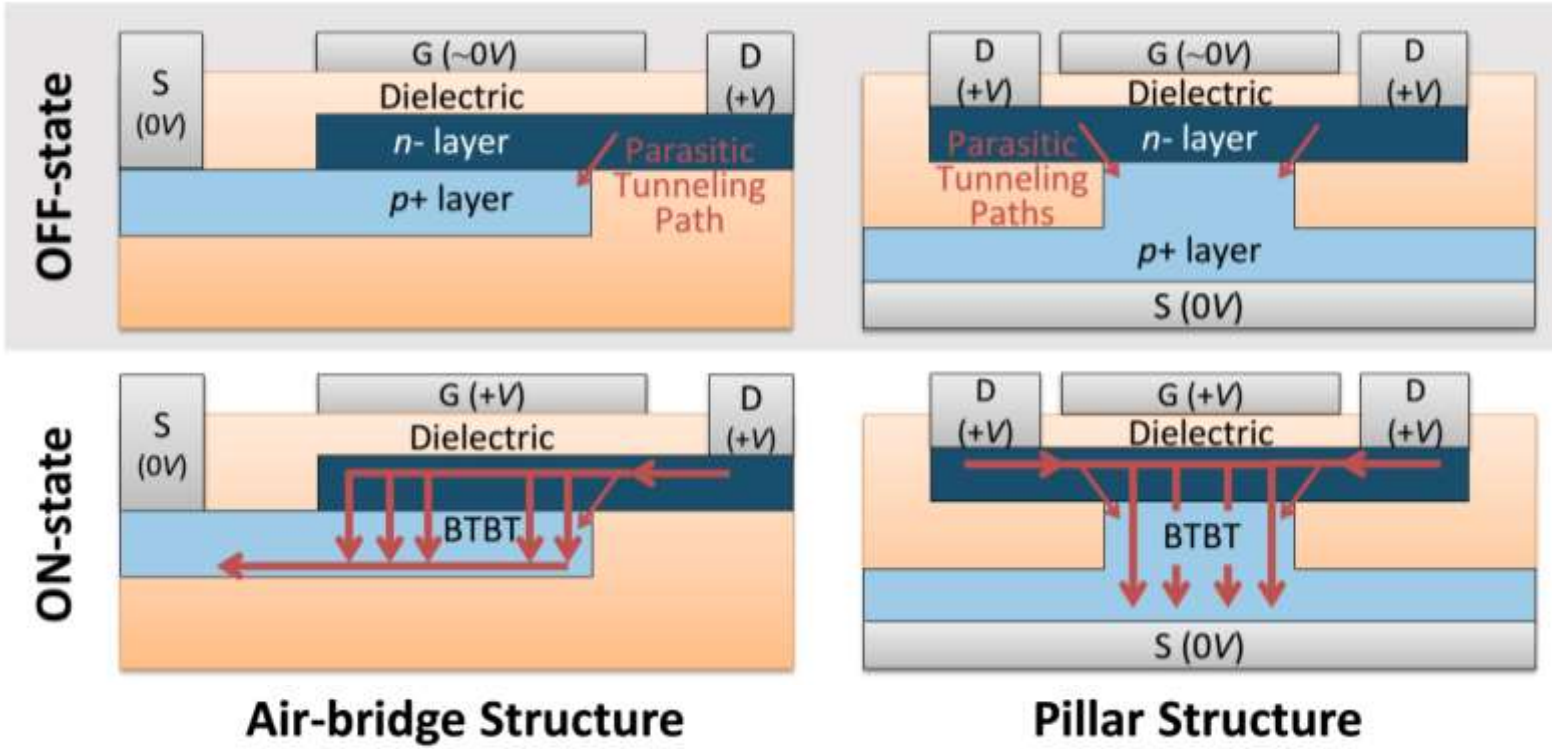


S. Agarwal and E. Yablonovitch, "Pronounced Effect of pn-Junction Dimensionality on Tunnel Switch Sharpness," 2011.

Vertical TFET Structures (1/2)

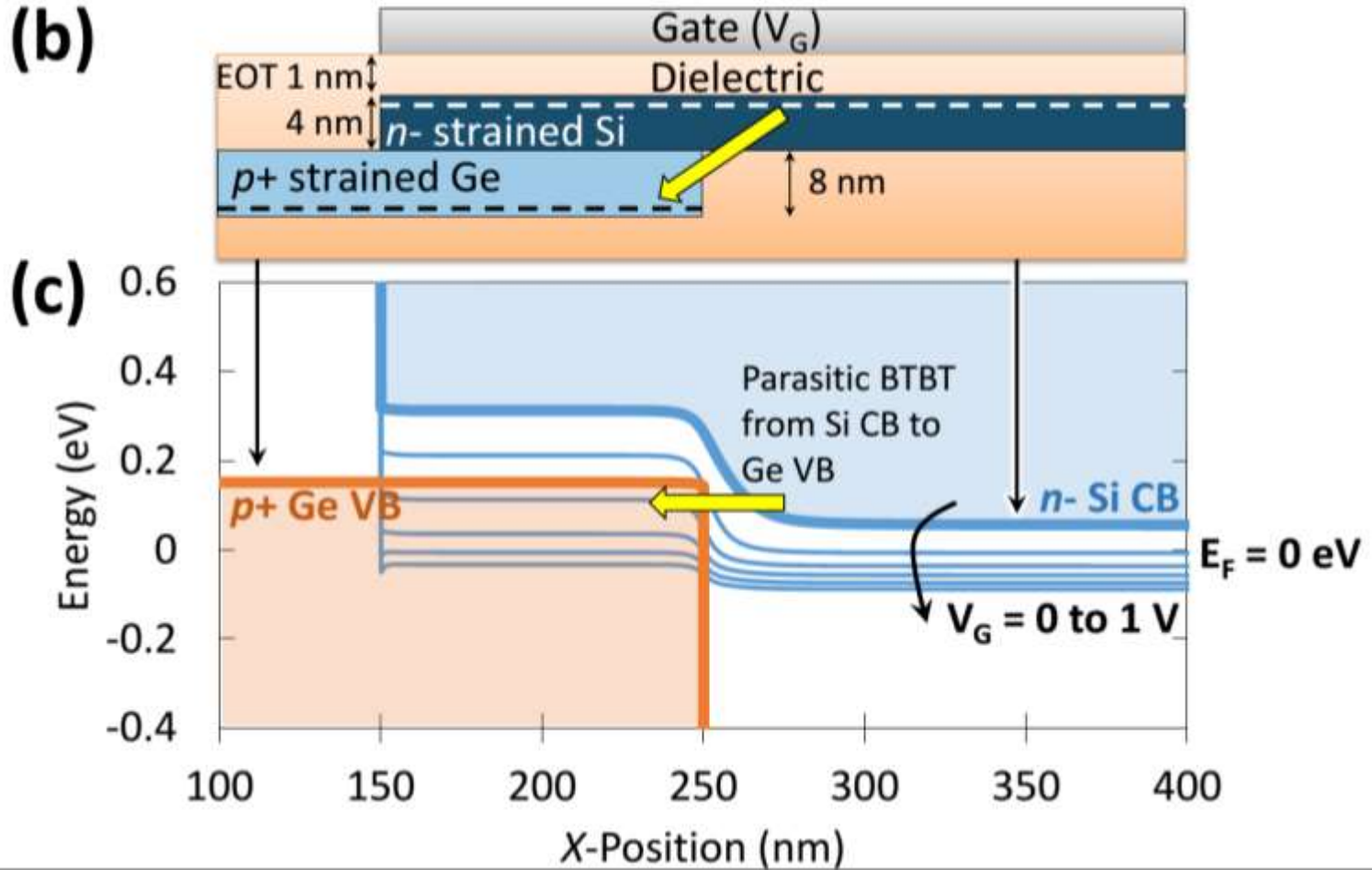


Vertical TFET Structures (2/2)

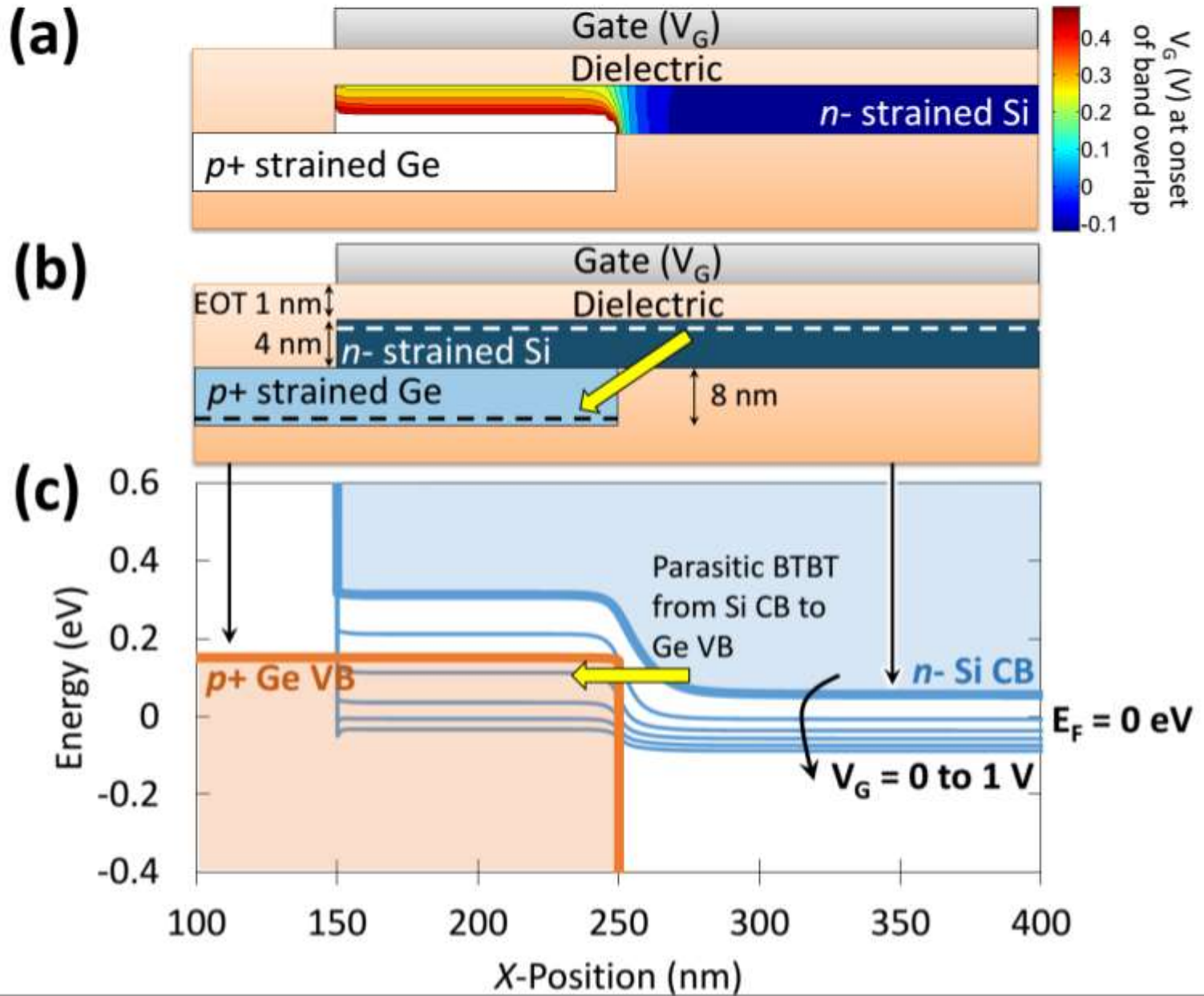


Parasitic diagonal tunneling paths can limit the off-state AND degrade the switching performance.

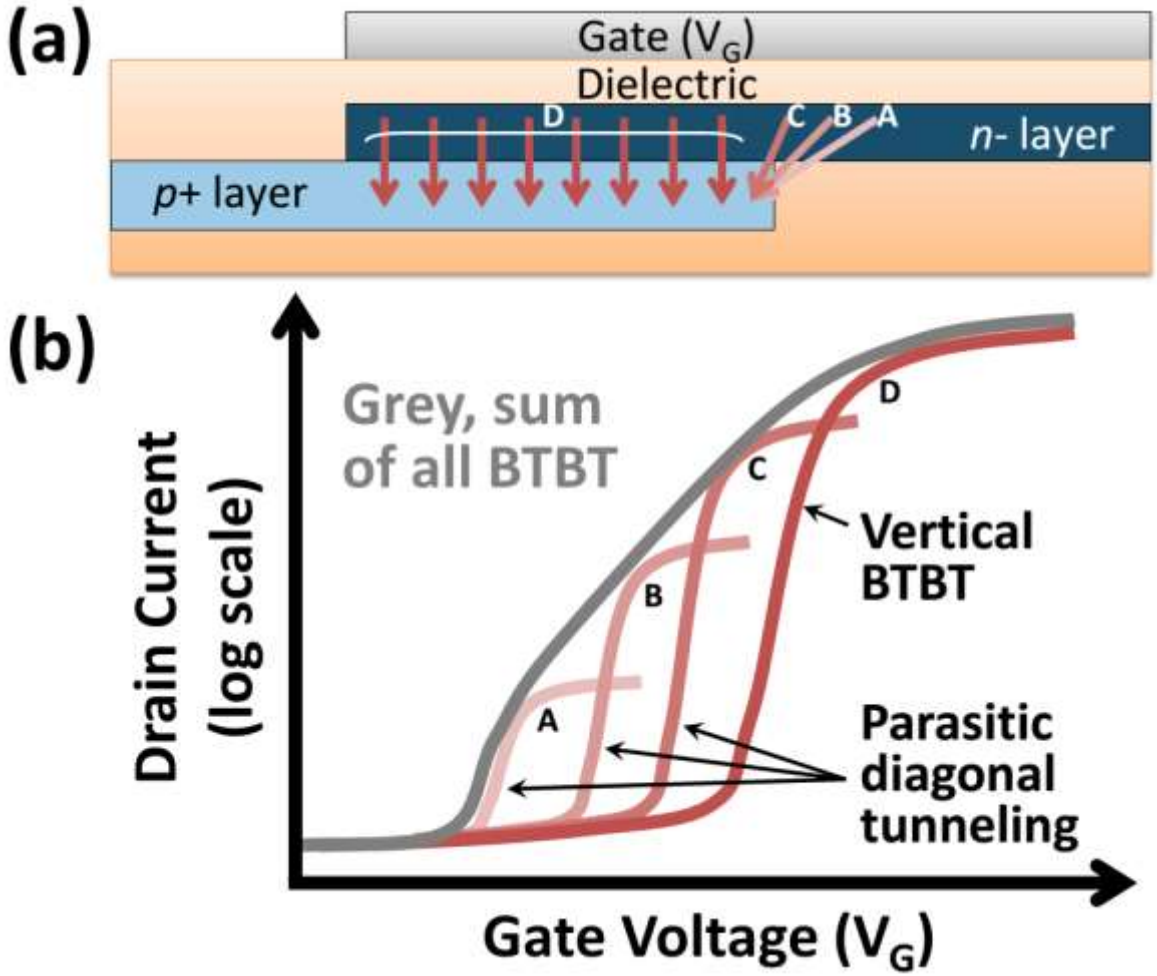
Parasitic Tunneling Paths (1/2)



Parasitic Tunneling Paths (2/2)

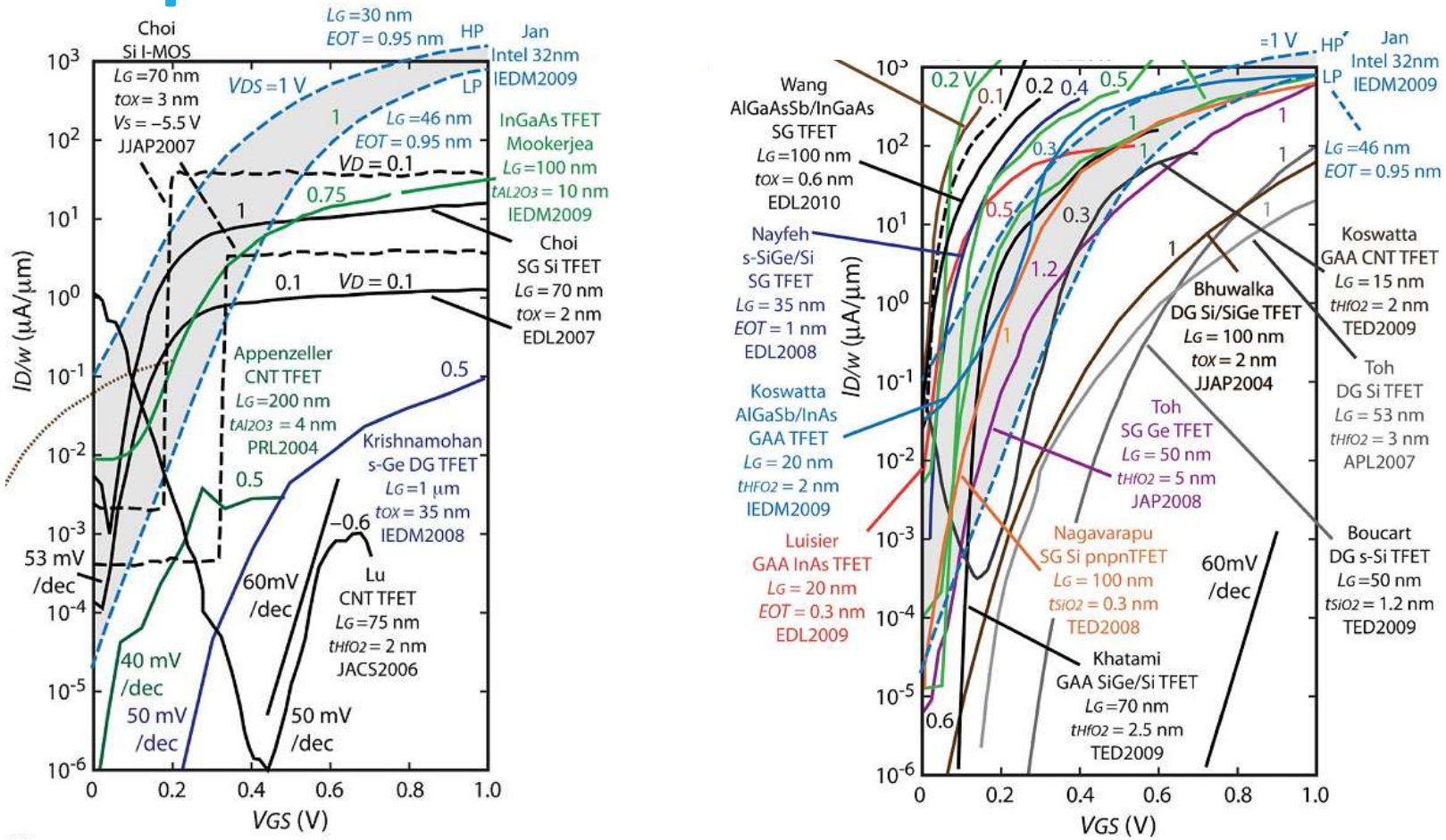


Impact of Parasitic Tunneling Paths



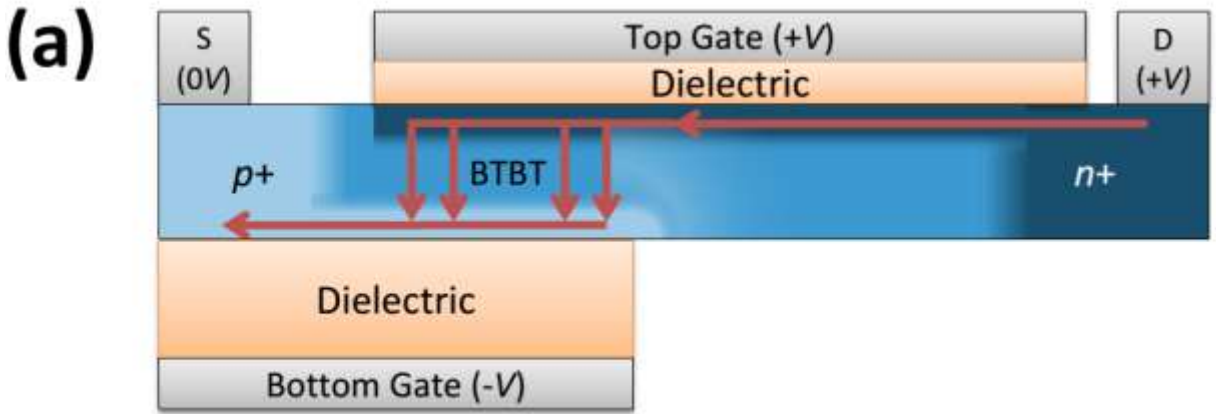
Though **D** is the desired tunneling path, parasitic paths **A**-**C** significantly reduce the sharpness of the turn-on (akin to varying threshold voltage).

Discrepancy between TFET **Experiments** and **Simulations**



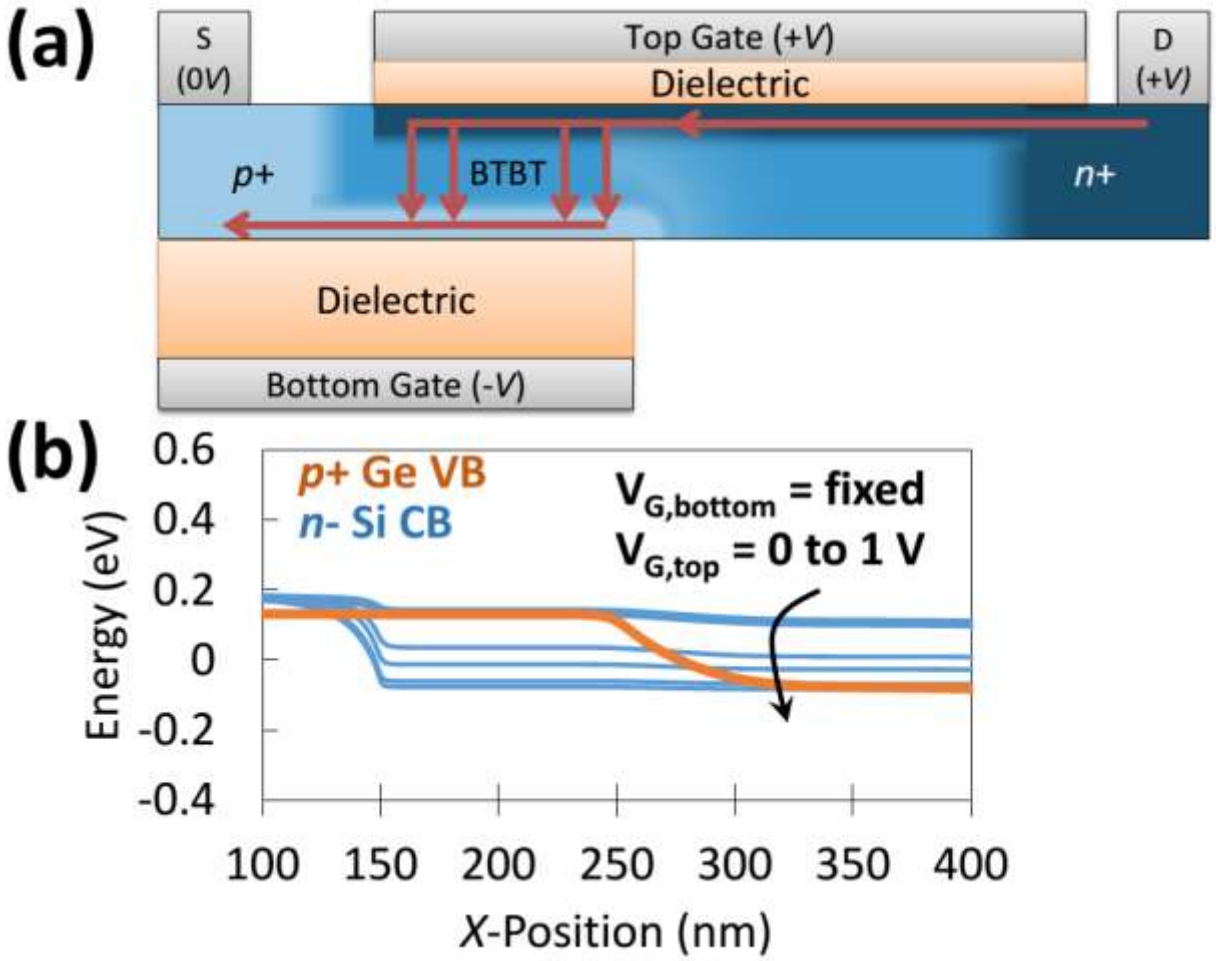
Seabaugh and Zhang, TED 2010.

Electrostatically-doped Vertical Bilayer TFET (1/2)



- No doping in channel region
  - Top gate accumulates electrons
  - Bottom gate accumulates holes
  - Carriers inherently aligned with gates
- Eliminates problems caused by doping
  - Band-tails
  - Dopant diffusion
  - Implant damage
- Eliminates parasitic paths (improved electrostatic design)

Electrostatically-doped Vertical Bilayer TFET (2/2)



Lateral electric field can be greatly reduced using thick bottom oxide
→ reduced parasitic diagonal tunneling

Summary

- The vertical TFET is an attractive structure but faces difficulties with electrostatic control of the channel
- A diagonal parasitic tunneling path can severely diminish both off-state and turn-on characteristics
  - Structure must be designed to prevent this parasitic path
- We plan to use the bilayer TFET to study tunneling device physics of fundamental switching abruptness