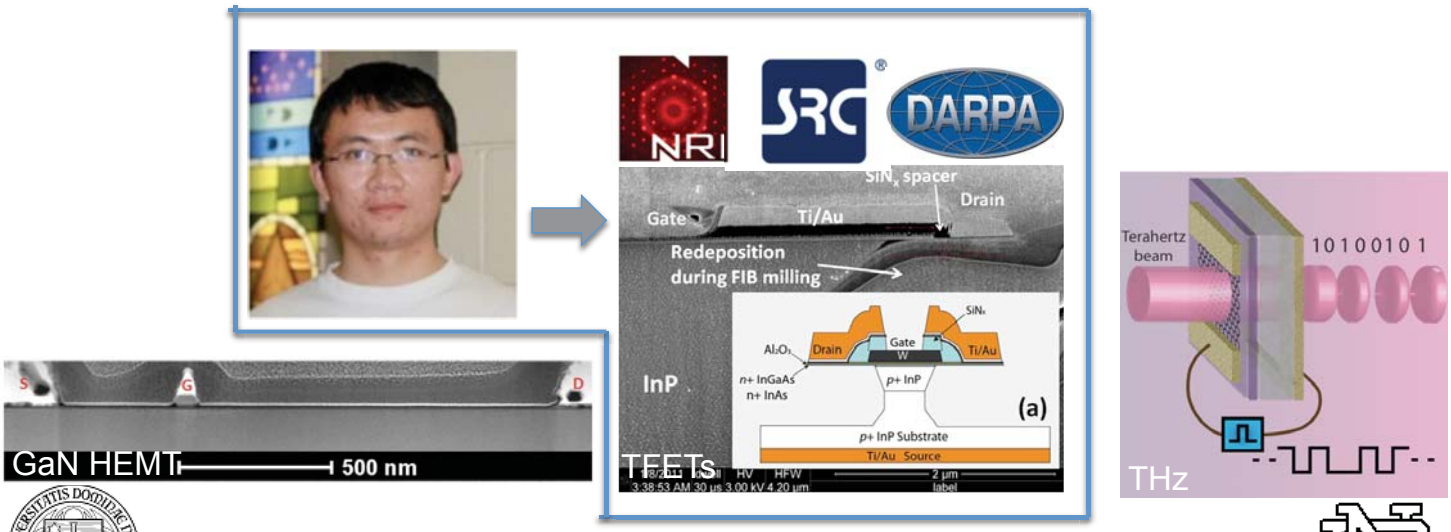
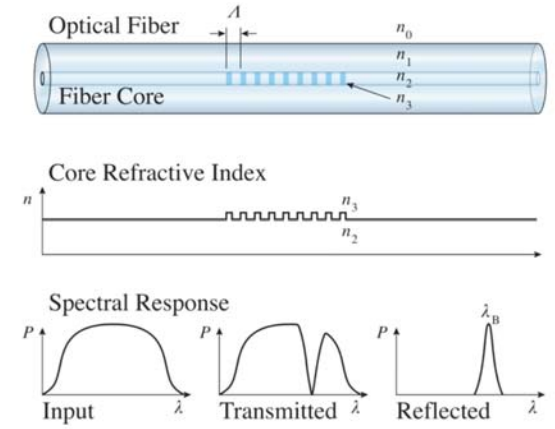
Tunnel FETs with tunneling normal to the gate

Huili Grace Xing

Students / postdocs: Guangle Zhou, Mingda Oscar Li, Yeqing Lu, Rui Li,
Faculty: Mark Wistey, Patrick Fay, Debdeep Jena, Alan Seabaugh
Electrical Engineering Department, University of Notre Dame



About me



Distributed Bragg Reflector

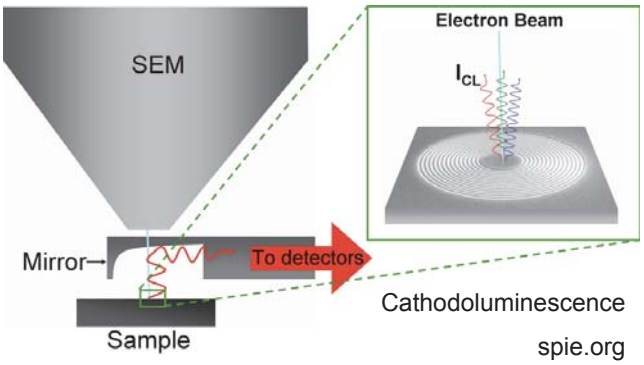
Wikipedia.com

Excimer laser illuminating through an optical mask on hydrogenated silica optical fiber

Physics (BS)

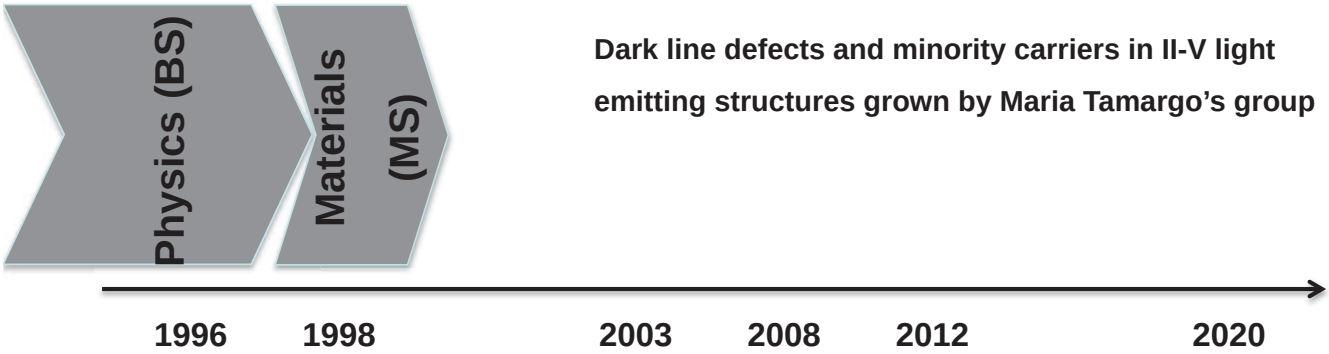
1996 1998 2003 2008 2012 2020

About me



Cathodoluminescence

spie.org

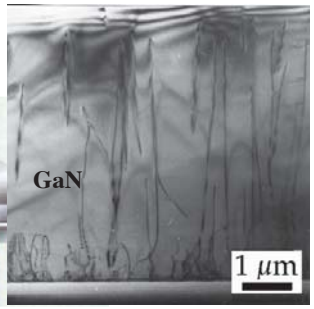


Dark line defects and minority carriers in II-V light emitting structures grown by Maria Tamargo's group

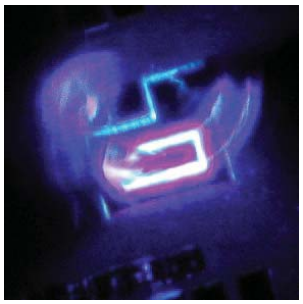
About me

GaN by MOCVD

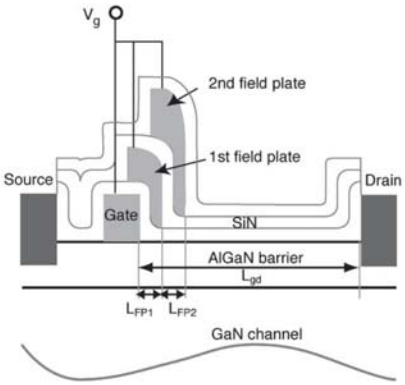
P-type doping



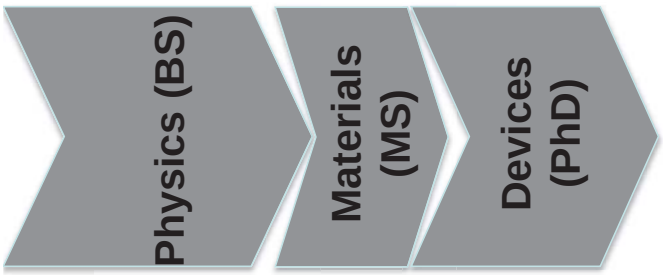
GaN HBT



GaN HEMT



GaN RF (GHz) and high speed power switches (MHz) – vertically integrated research



Devices: Mishra, Rodwell

Physics: Kroemer, Jena

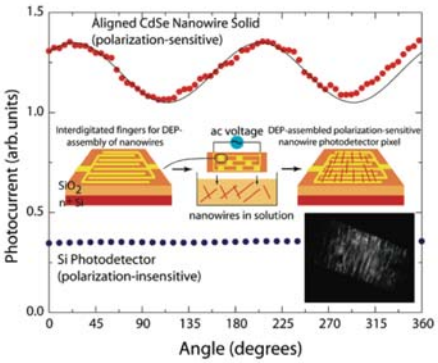
Materials: Speck, DenBaars

Nanofabrication: Evelyn Hu

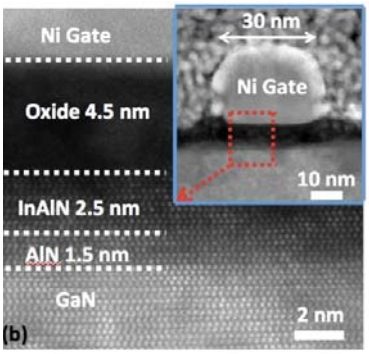
1996 1998 2003 2008 2012 2020

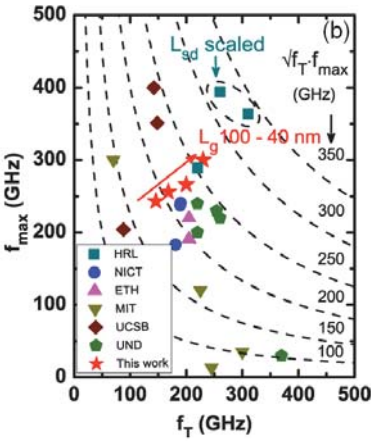
About me

Nanowires: FETs, photodetectors



GaN RF, high speed power switches, wafer bonding

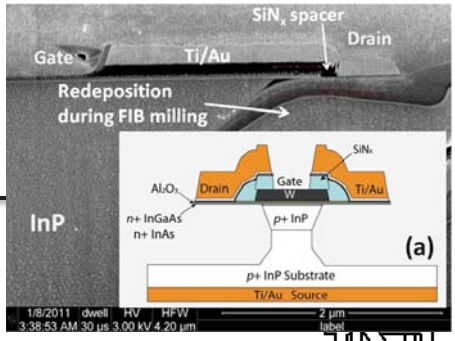




Physics (BS) → Materials (MS) → Devices (PhD) → Start GaN, nano, TFET at UND

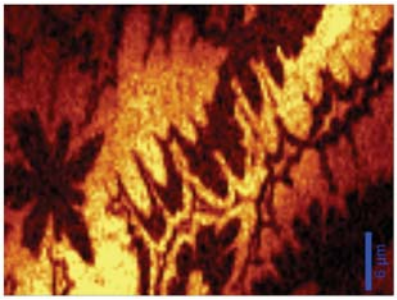
1996 1998 2003 2008 2012

Tunnel FETs

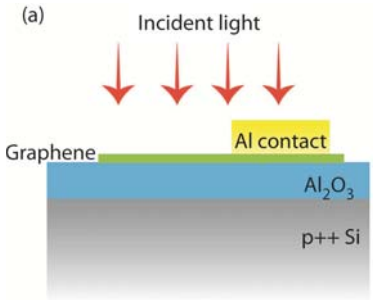


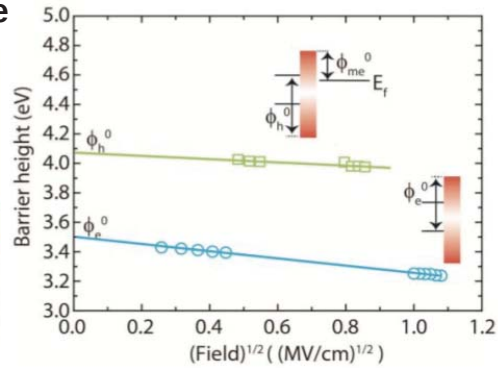
About me

Isotope labeled graphene



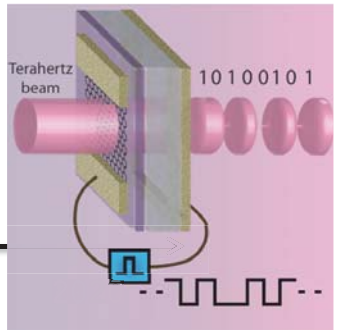
Band diagram determination by IPE enabled by optical transparency of graphene





1996 1998 2003 2008 2012

THz modulators

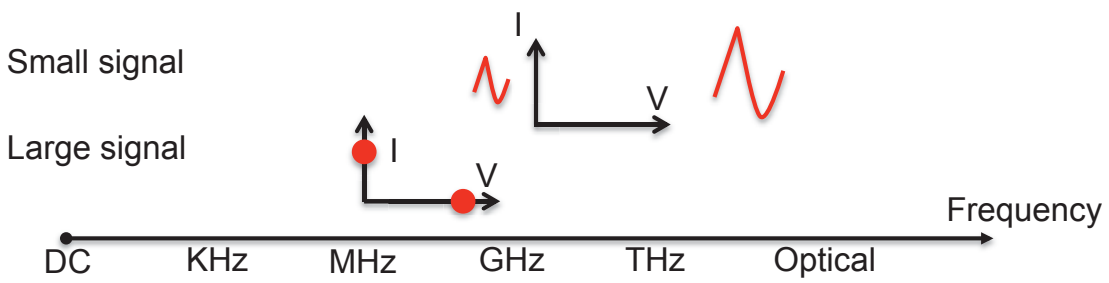


Research interests

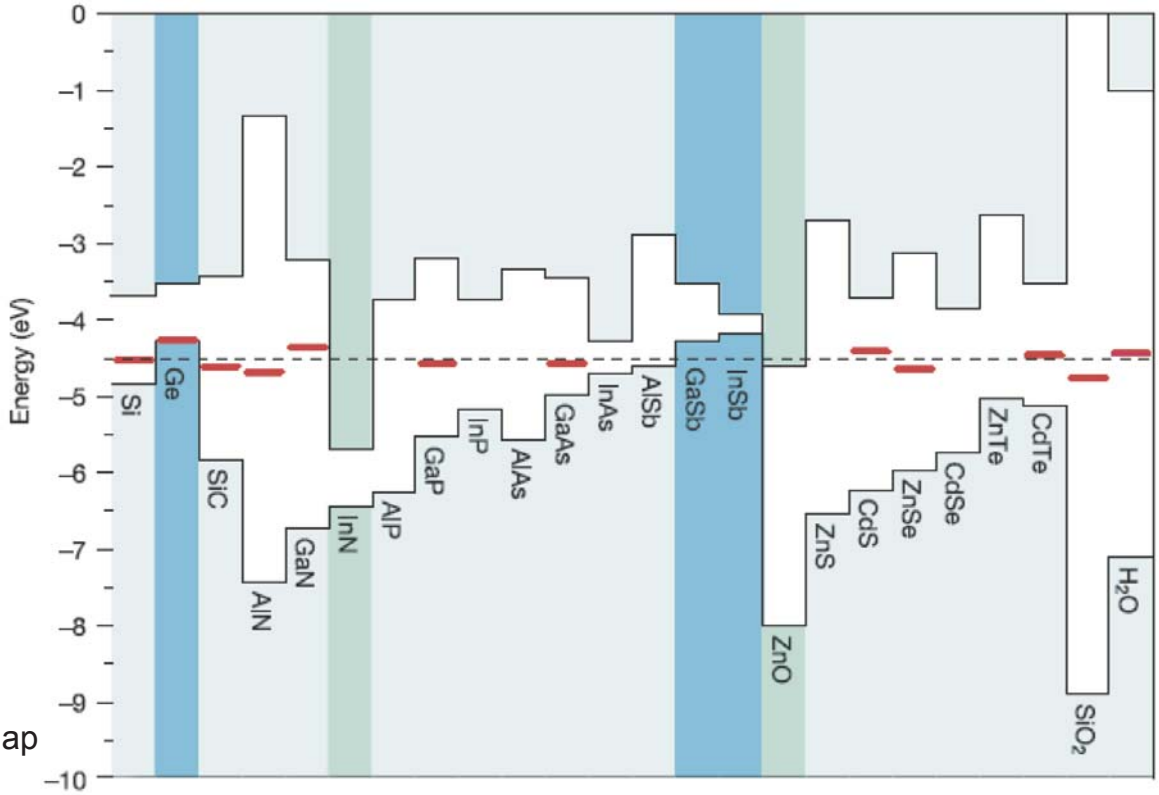
RF Electronics | *Electronic switch for power and computation* | *Photonics*

New Materials *New Physics* *New Device Ideas*

Right choice of materials → high performance devices



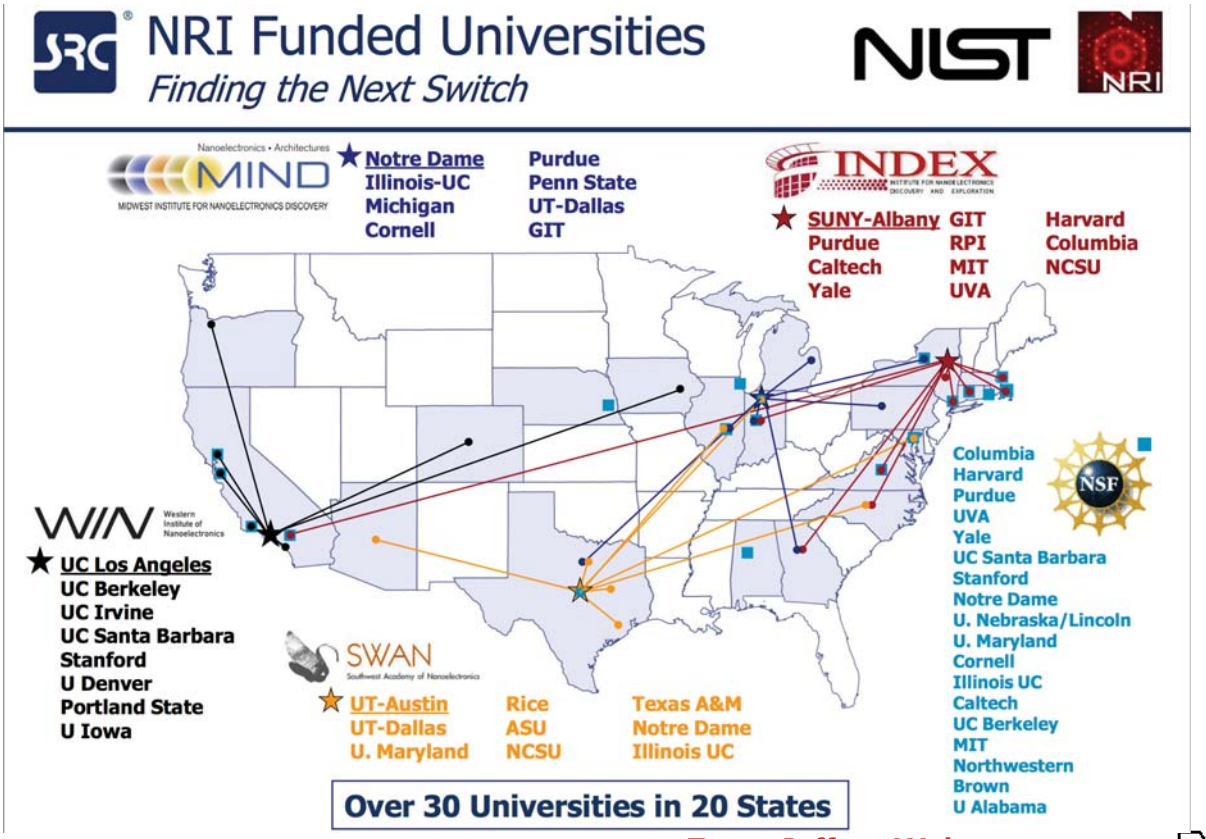
The materials world



A partial map

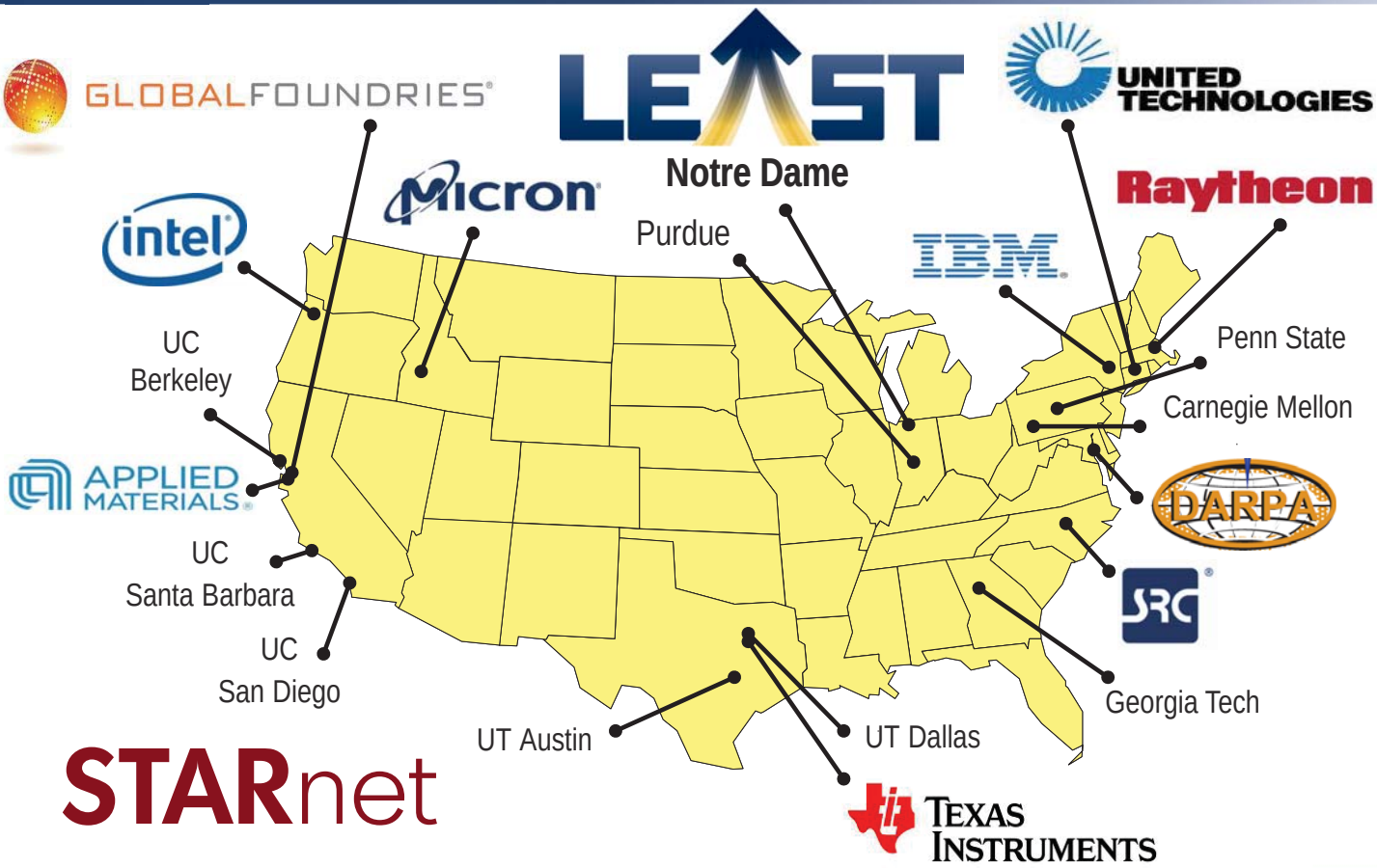
Chris Van de Walle, J. Neugebauer, Nature 2003
Universal alignment of hydrogen levels in semiconductors, insulators and solutions

The Project on next generation electronic switch



From Jeffrey Welser
NRI 1.0 and 1.5 Director

10 universities – 26 principal investigators – supporting network



Courtesy of seabaugh.1@nd.edu

Focus Center Research Program – STARnet

STARnet Mission: To develop next-generation microelectronics to maintain U.S. leadership in semiconductor technology vital to U.S. prosperity, security and intelligence.

Center for Low Energy Systems Technology at the University of Notre Dame – Director Alan Seabaugh

Center for Function Accelerated nanoMaterial Engineering (FAME) at UCLA – Director Jane Chang

Center for Spintronic Materials, Interfaces and Novel Architectures at U. Minn. – Director Jian-Ping Wang

Center for Future Architectures Research at the University of Michigan – Director Todd Austin

Center for Systems on Nanoscale Information Fabrics at UIUC – Director Naresh Shanbhag

TerraSwarm Research Center at the University of California, Berkeley – Director Edward Lee

STARnet

DARPA
Applied Materials
GLOBALFOUNDRIES
IBM
Intel Corporation
Micron Technology
Raytheon
Texas Instruments
United Technologies

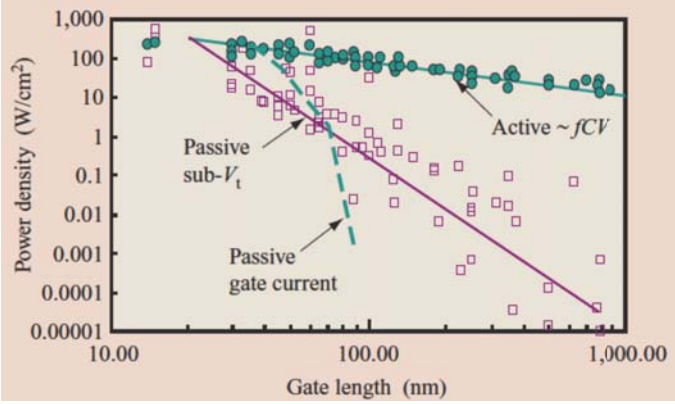
Courtesy of seabaugh.1@nd.edu

Center mission and motivation

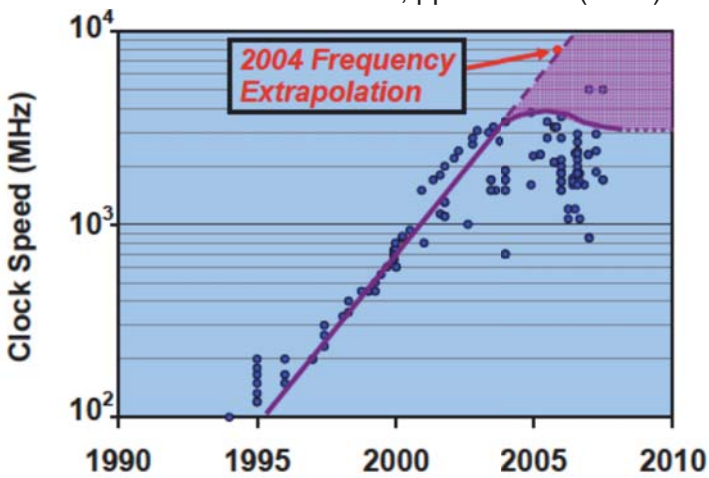
Re-enable voltage scaling by demonstrating devices with subthreshold swing less than 60 mV/decade

Move VLSI technology beyond limits associated with power density

Map out digital, analog, and mixed signal applications for steep, low voltage devices



Haensch et al. IBM J. R&D. 50, pp. 339-361 (2006).



Haensch 2008

Midwest Institute for Nanoelectronics Discovery

MIND


Gary Bernstein

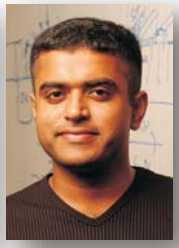

György Csaba


Suman Datta


Patrick Fay


Sharon Hu


Wan Sik Hwang


Debdeep Jena


Jiyoung Kim


Gerhard Klimeck


Peter Kogge


Tom Kosel

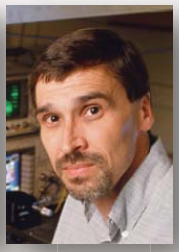

Theresa Mayer


Joe Nahas


Vijay Narayanan


Michael Niemier


Wolfgang Porod

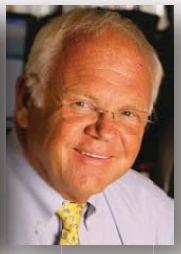

Alan Seabaugh


Robert Wallace


Mark Wistey


Grace Xing

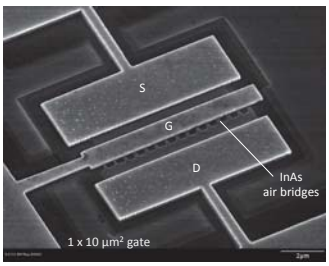

Qin Zhang


Robert Dunn

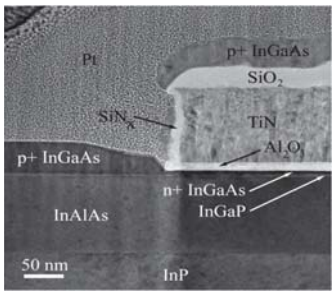

Heidi Deethardt

III-V tunnel field-effect transistors (TFET)

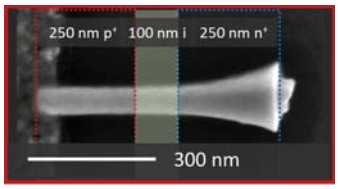
Demonstration of gate placement options



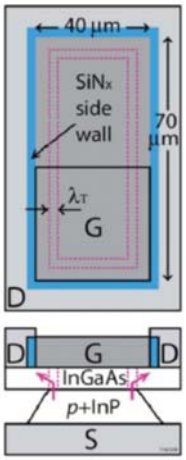
in-line, air-bridge drain



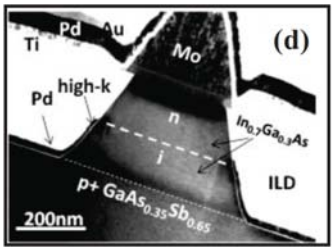
regrown tunnel junction



nanowire *p-i-n* TFET

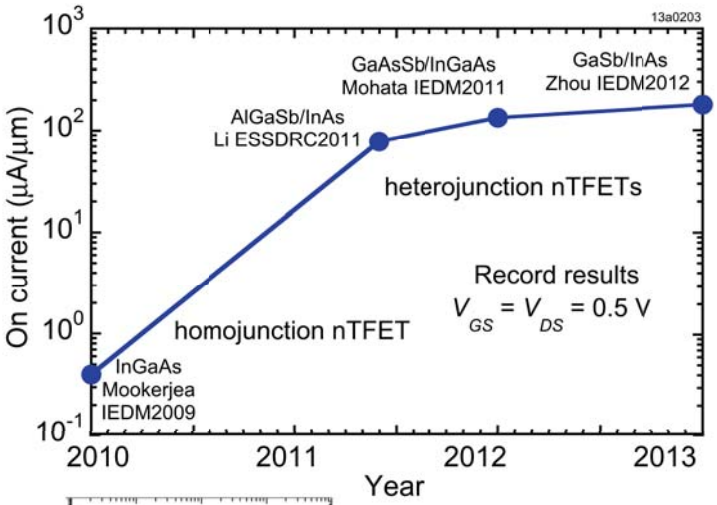


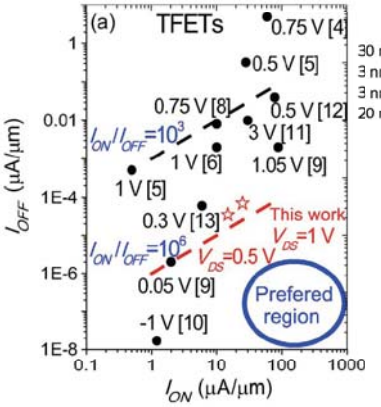
in-line, self-aligned, gate first & gate-last TFETs

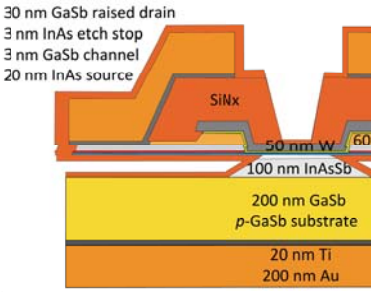


sidewall-gate HJ TFET

Advance of TFET on-current in MIND

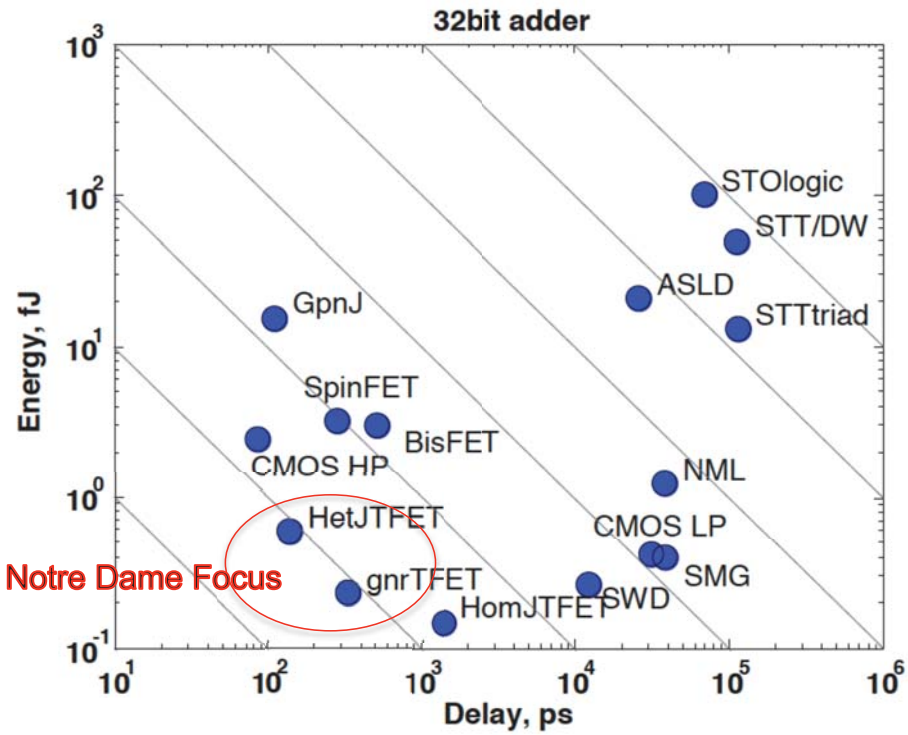






GaSb/InAs *p*-~~TF~~ET~~s~~

Snapshot of competing technology in 2012



Nikonov and Young, Proceedings of IEEE (2013)
Uniform methodology for benchmarking beyond-CMOS devices, 2012
arXiv:1302.0244 [pdf]

TFET 101

n- TFET

Thermal tail is small due to the bandgap filtering thus TFETs are not fundamentally limited by the thermionic emission process in MOSFETs.

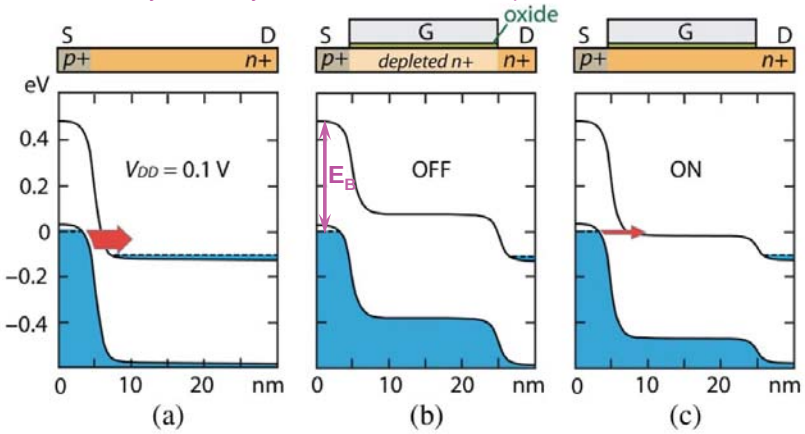
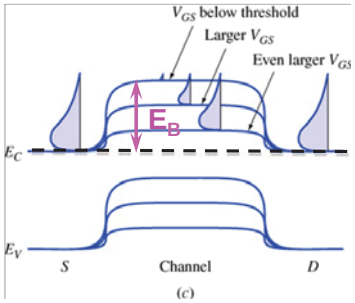


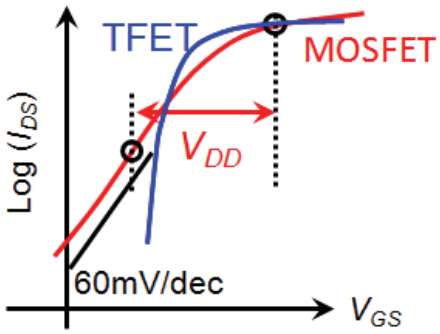
Fig. 1. ***Energy band diagram and layer structure for an nTFET consisting of an n^+ source (S), p^+ drain (D), and gate (G). In (a) the Zener tunneling p^+n^+ channel is shown under 0.1-V bias without a gate. In (b), the gate fully depletes the channel at zero gate potential creating a normally off device. In (c), a positive gate voltage turns the channel on with current set by the overlap of valence band electrons with unfilled conduction band states.***

A. Seabaugh and Q. Zhang, Proceedings of the IEEE, 98(12), 2095 (2010)

n- MOSFET

Thermal tail is responsible to the subthreshold current





Anderson & Anderson, Fundamentals of Semiconductor Devices, McGraw Hill (2005)

Why steep SS promised in TFETs: dimensionality, materials choices

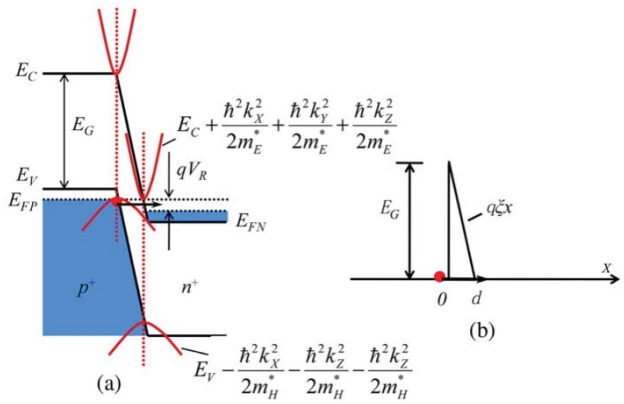
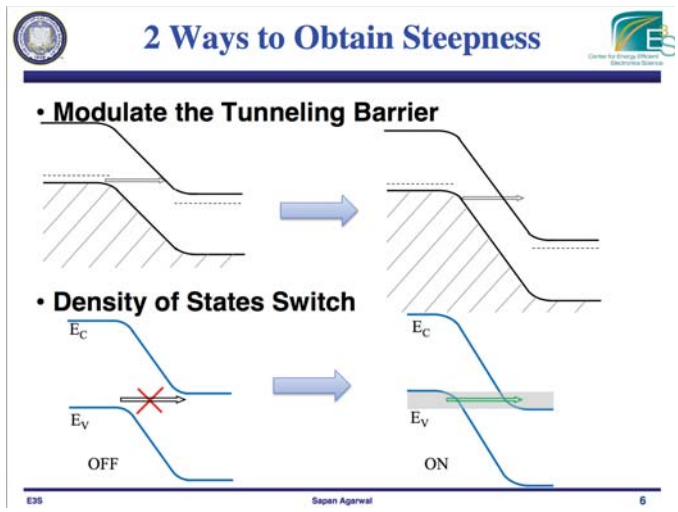


Fig. 4. ***(a) Zener tunneling in a reverse-biased p^+n^+ junction for bulk semiconductors and (b) the triangular potential barrier seen by electrons tunneling in the x-direction.***



Requirement: excellent electrostatic control (similar to MOSFETs)
Result: $S \sim 2.3 * V_{GS}$ + 2nd term.

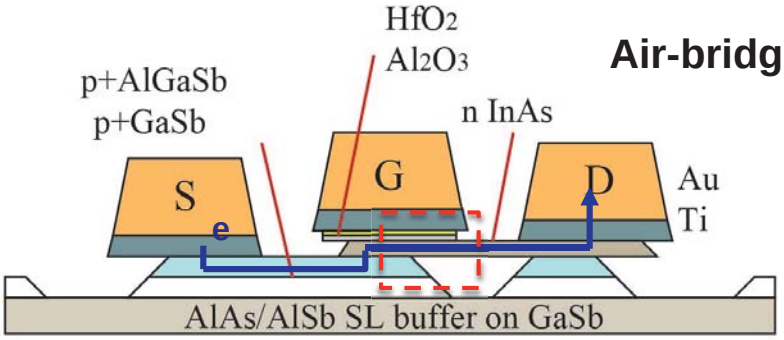
Requirement: V_{GS} efficiently vary electric field along the tunnel direction
Result: better to align tunnel direction ⊥ to the gate.

$$J^{3D} = \frac{\sqrt{2m_R^*}q^3\xi V_R}{8\pi^2\hbar^2 E_G^{1/2}} \exp\left(-\frac{4\sqrt{2m_R^*}E_G^{3/2}}{3q\xi\hbar}\right). \quad (5)$$

$$S = \ln(10)\left[\frac{1}{V_R}\frac{dV_R}{dV_{GS}} + \frac{\xi + b}{\xi^2}\frac{d\xi}{dV_{GS}}\right]^{-1}. \quad (12)$$

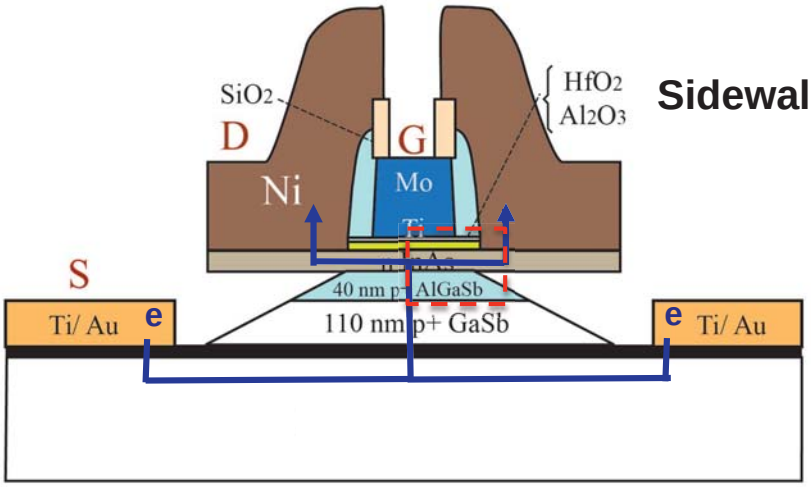
A. Seabaugh and Q. Zhang, Proceedings of the IEEE, 98(12), 2095 (2010)

Experimental approaches

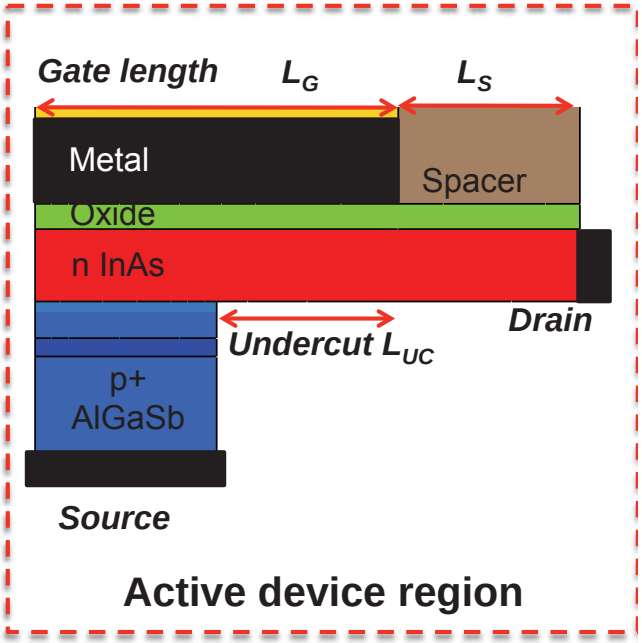


Air-bridge

- as-grown heterojunction
- 2D channel (5-10 nm InAs)

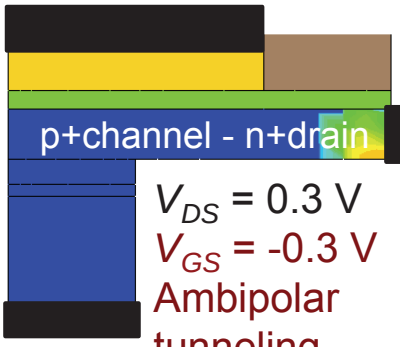


Sidewall

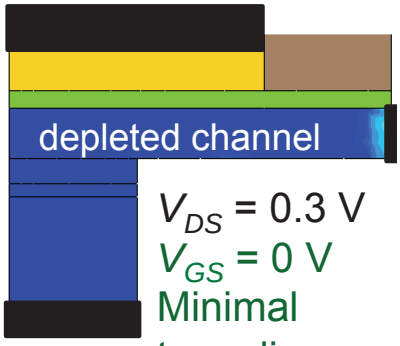


Active device region

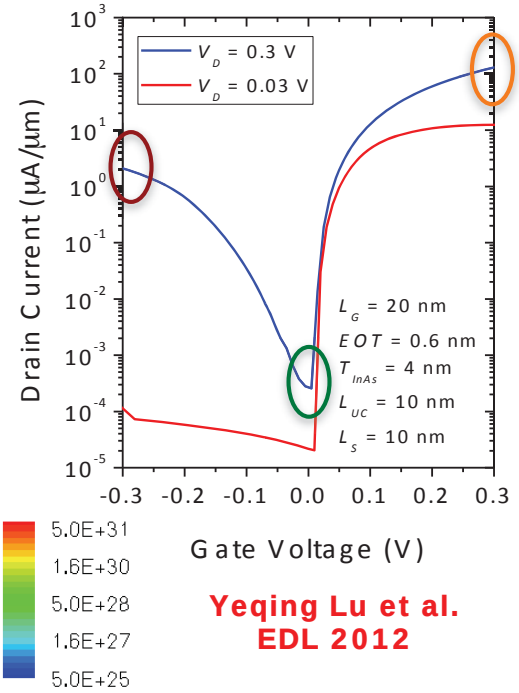
Physics of in-line TFET



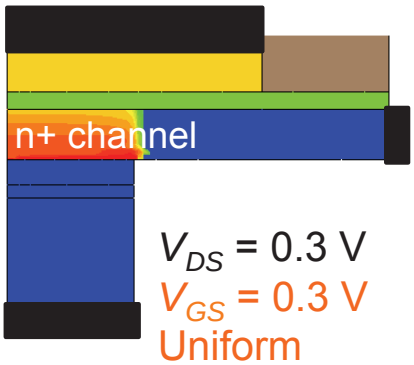
V_{DS} = 0.3 V
V_{GS} = -0.3 V
Ambipolar tunneling current



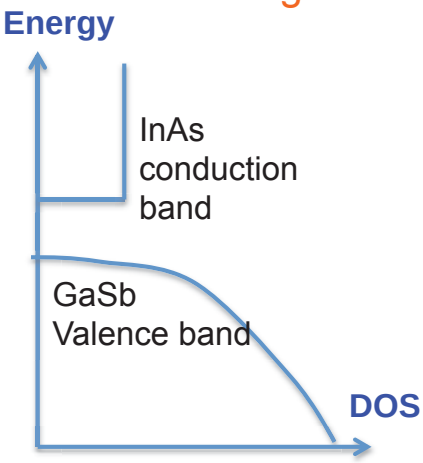
V_{DS} = 0.3 V
V_{GS} = 0 V
Minimal tunneling



Yeqing Lu et al. EDL 2012

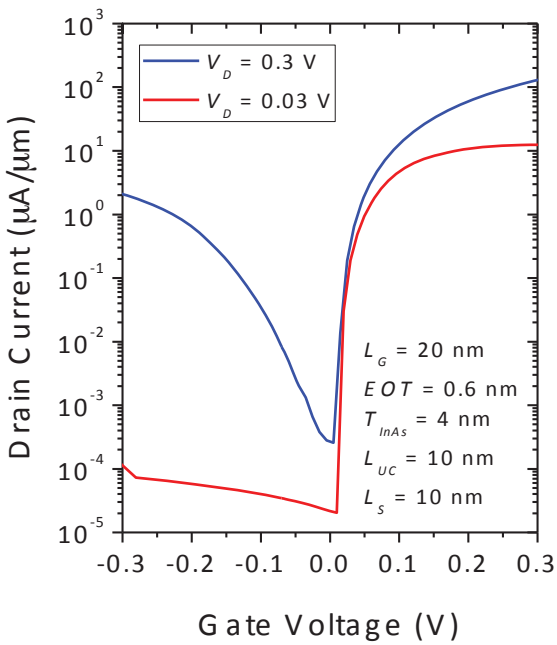


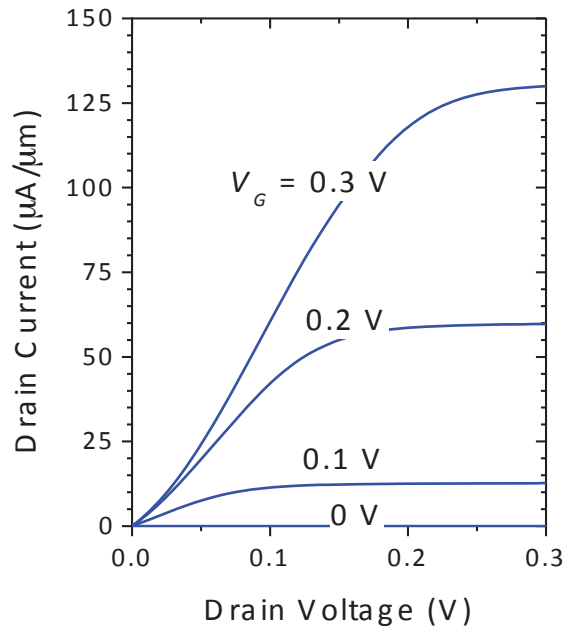
V_{DS} = 0.3 V
V_{GS} = 0.3 V
Uniform tunneling



Common source characteristics

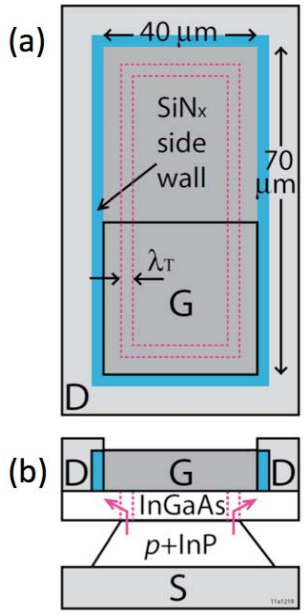
Synopsis TCAD 2010.03

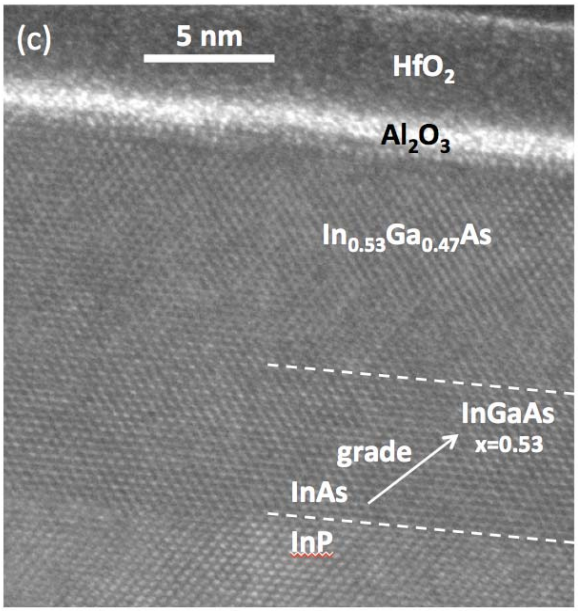




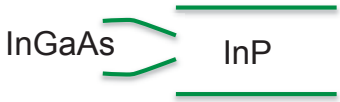
Negligible threshold voltage shift between V_D = 0.3 and 0.03 V, indicating no obvious drain induced barrier lowering in this designed structure.

$In_{0.53}Ga_{0.47}As/InAs/InP$ VTFET (straddling)





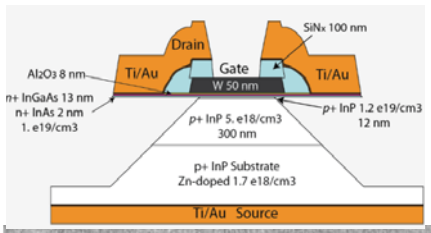
- Remove epi-cap
- Deposit high K dielectric
- Deposit W gate and SiN
- Dry etch W/SiN
- Form SiN sidewall
- Deposit Drain Contact
- Pattern and open Gate Pad
- Deposit Source Contact
- Selective wet etch n-In(Ga)As
- Selective wet undercut etch p-InP
- ALD passivation (optional)

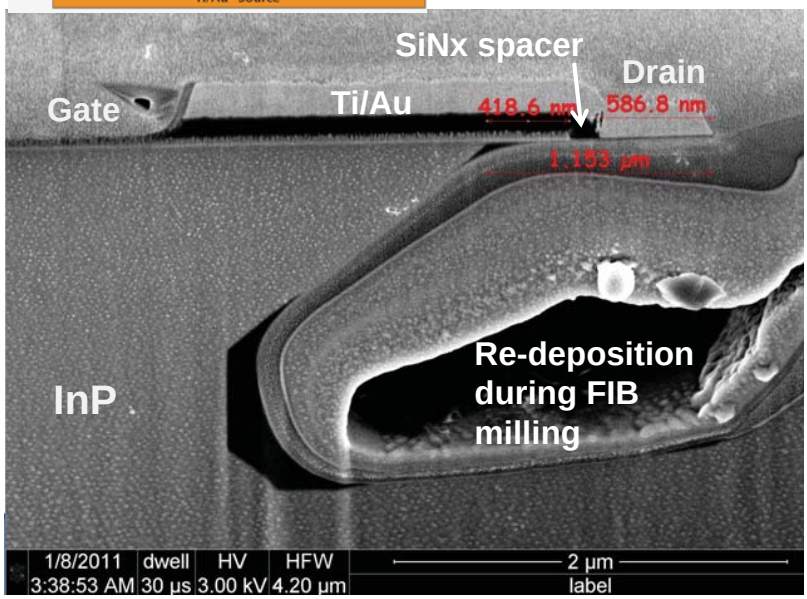


Advantages:
- No regrowth needed
- Self-aligned drain-to-gate
- P+ substrate enables simple fabrication
- Better electrostatics for low subthreshold swing

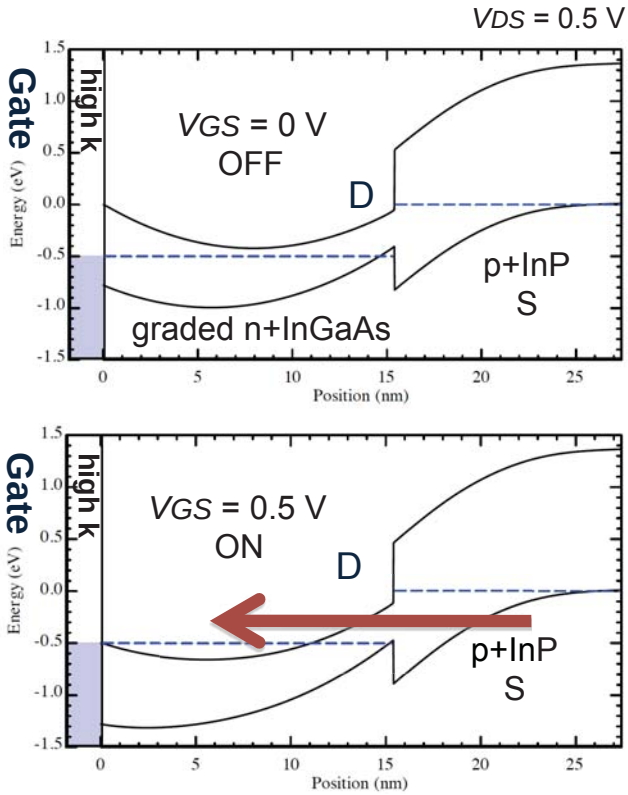
Guangle Zhou et al, CSMantech 2011
Guangle Zhou et al, IEEE EDL 2011
Guangle Zhou et al, IEEE EDL 2012

$In_{0.53}Ga_{0.47}As/InAs/InP$ VTFET (1)





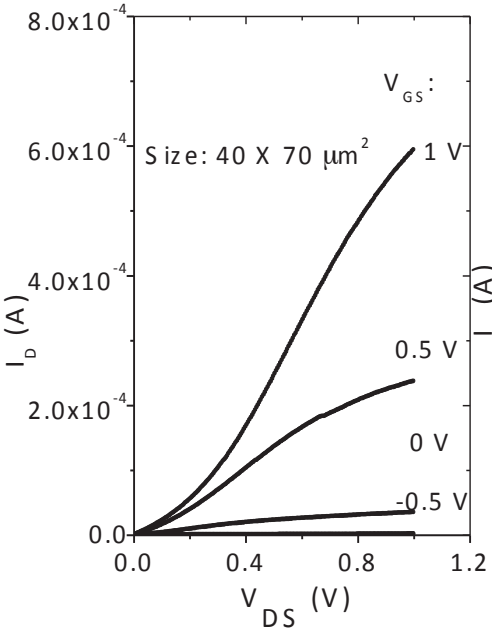
Guangle Zhou et al, CSMantech 2011

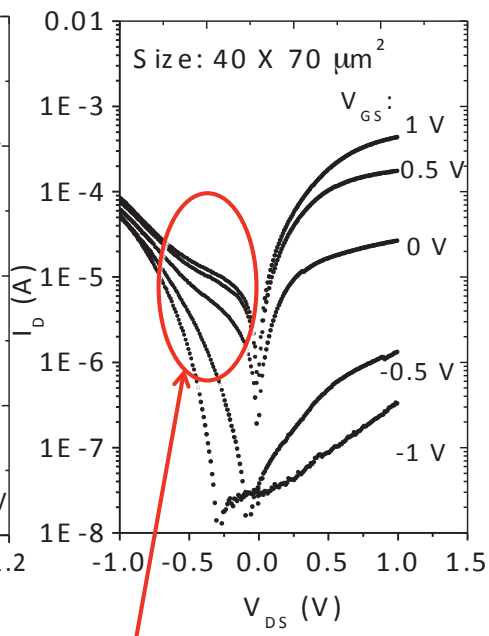


Energy band diagrams

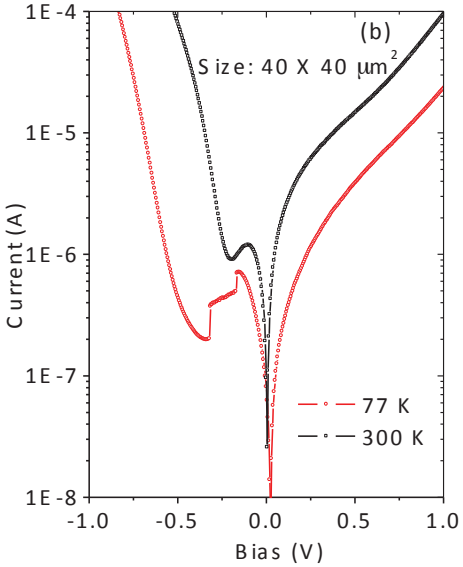
$In_{0.53}Ga_{0.47}As/InAs/InP$ VTFET (2)

Tunnel Transistors





Tunnel diodes



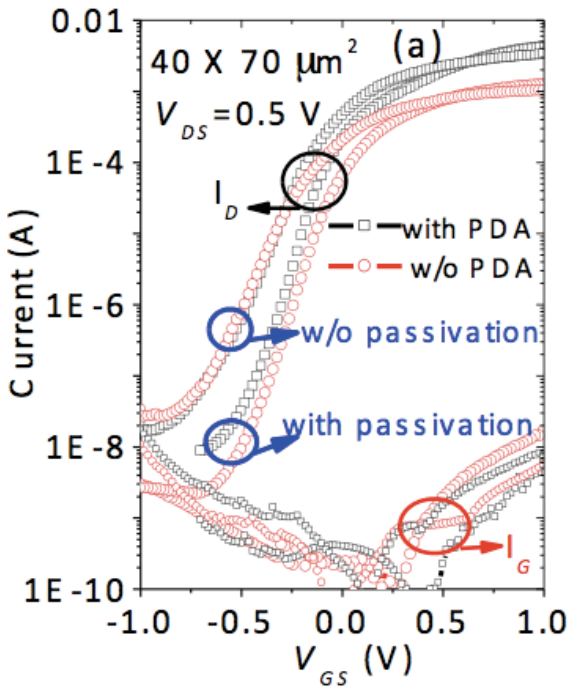
Modulation of Zener tunnel current

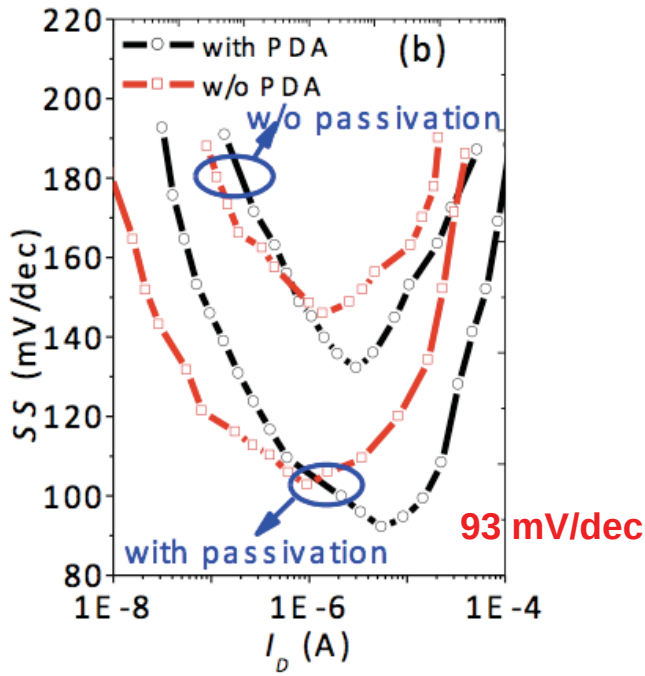
NDR trend under negative drain bias (forward biased p-n junction)

NDR observed in diodes
T-dep I-V indicates significant presence of trap states.

Guangle Zhou et al, CSMantech 2011 I_D-V_{DS} characteristics w/o PDA

$In_{0.53}Ga_{0.47}As/InAs/InP$ VTFET (4)



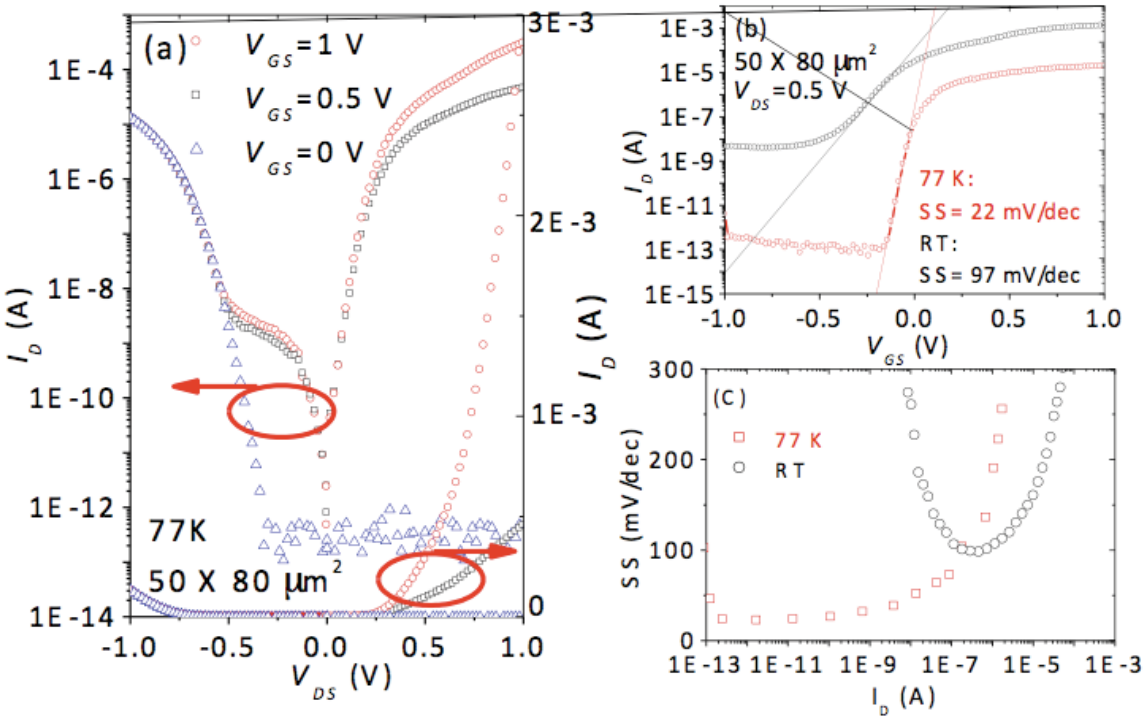


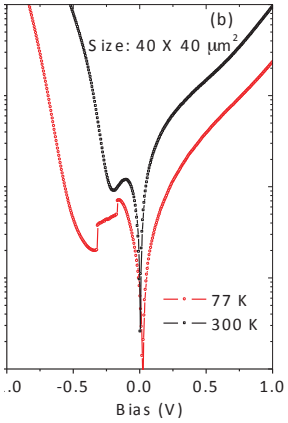
PDA: Al_2O_3 annealed at 350 °C for 3mins in N_2 ambient
Passivation: PECVD SiN 10 nm @ 120 °C

Both PDA and SiN passivation improved SS of TFET

Guangle Zhou et al, EDL 2012

$In_{0.53}Ga_{0.47}As/InAs/InP$ VTFET (6)

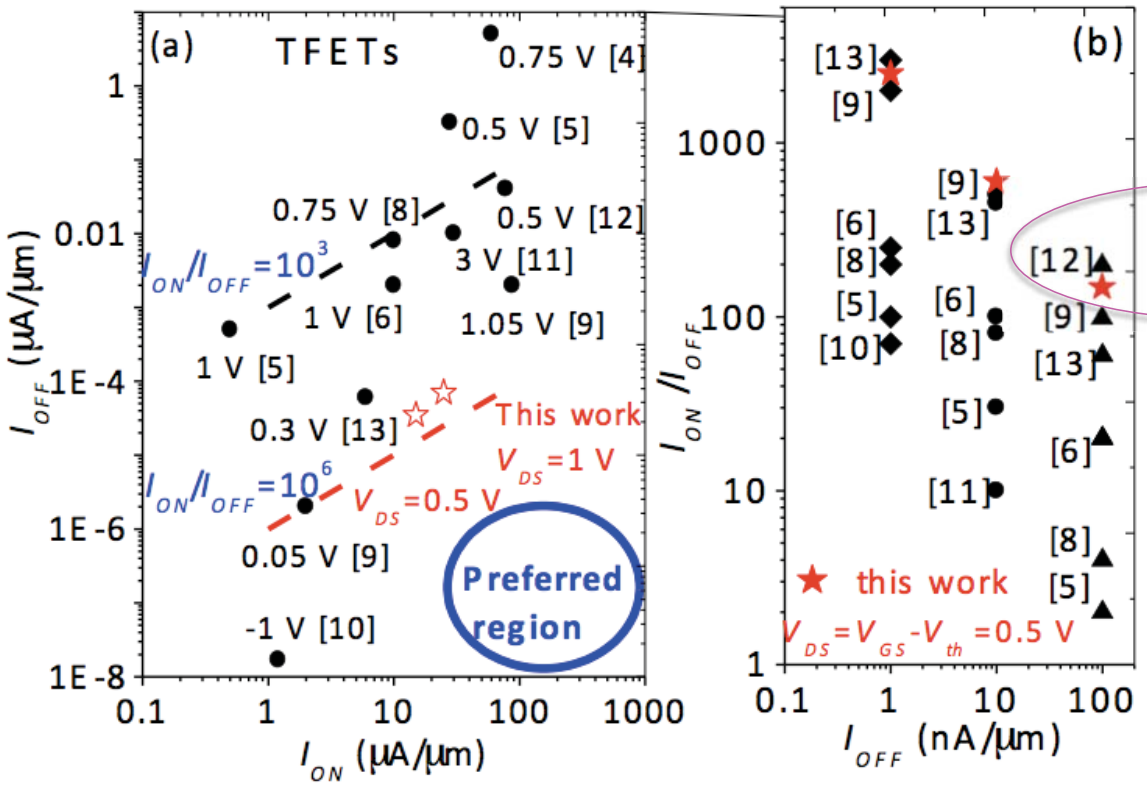




- SS decreased with Temp (most likely due to traps and Dit)
- NDR observed in diode both at 77 K and 300 K (thus device operates by tunneling)
- SS also limited by the electrostatics

Guangle Zhou et al, EDL 2012

III-V TFETs (by Spring 2012)

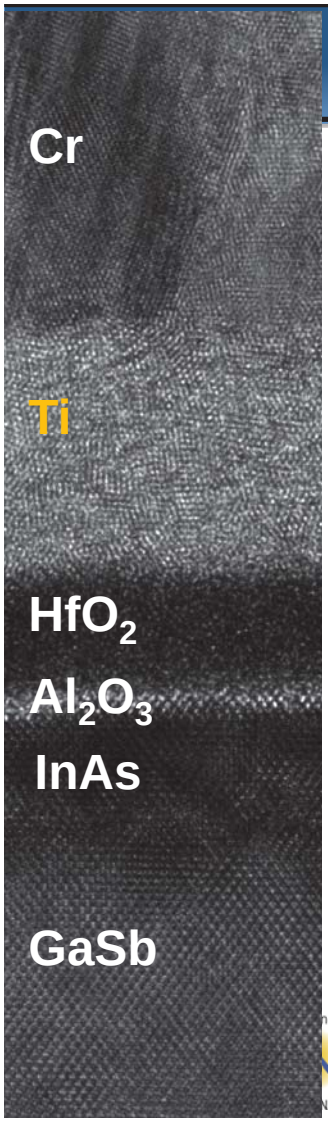


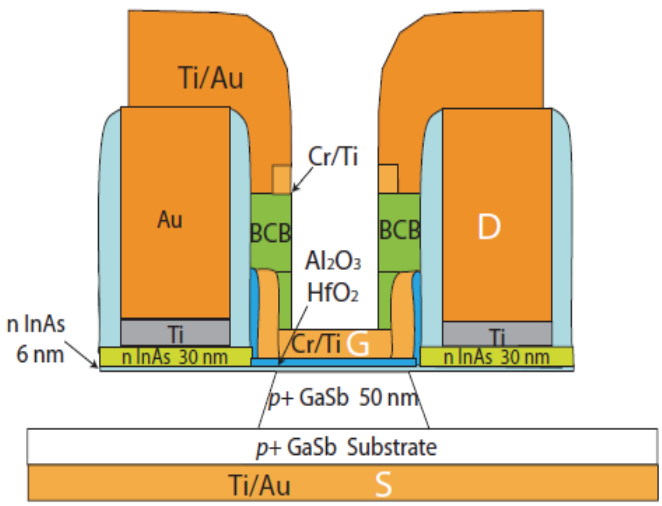
Higher current due to Tunneling aligned with gate field

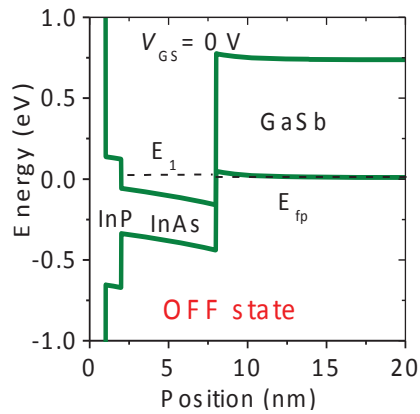
[9] H. Zhao et al, UTAustin, TED 2011
[12] Rui Li et al, UND, EDL 2012
[13] Dewey et al, Intel, IEDM 2011

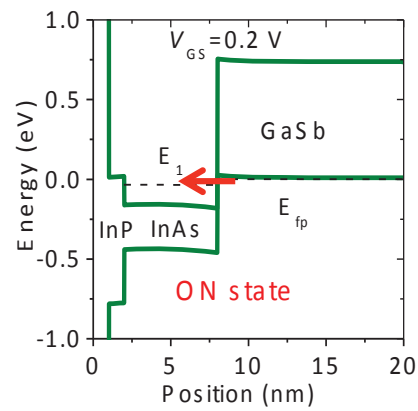
Guangle Zhou et al, IEEE EDL 2012

Sidewall p+GaSb/nInAs TFETs





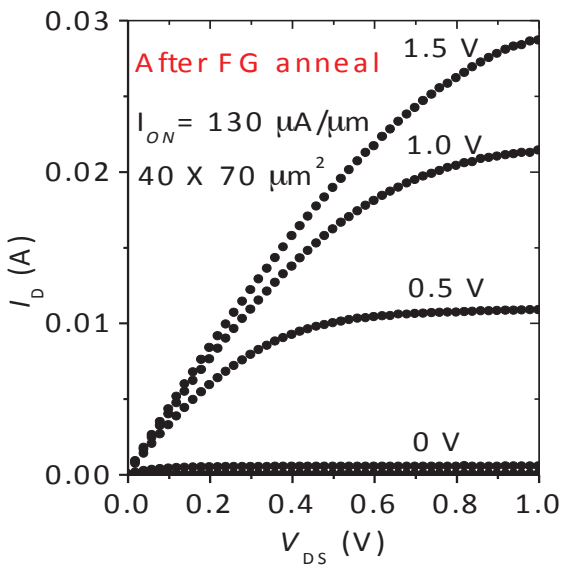


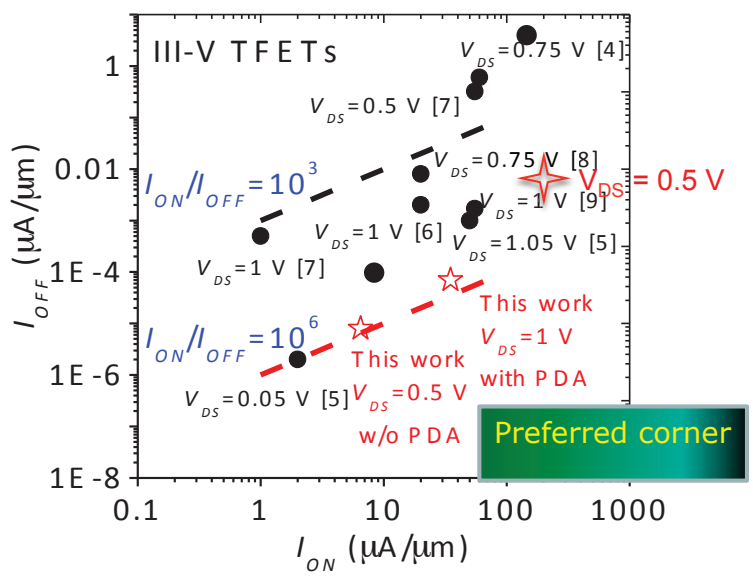


- Improved ohmic contacts
- Fully self-aligned process
- current carried equally by device periphery.

G. Zhou et al., *IEDM* (2012)

Sidewall p+GaSb/nInAs TFETs (near broken gap)

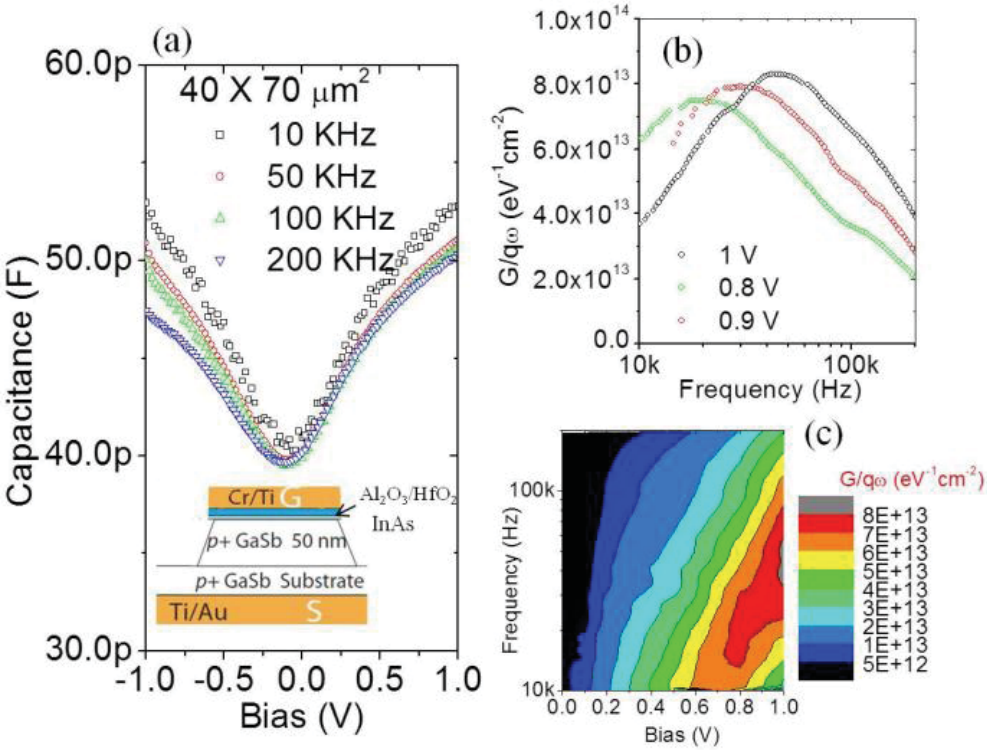




- DC: @ V_{DS}=0.5 V, I_{ON}= 105 μA/ μm, SS_{MIN}= 120 mV/dec, I_{ON}/I_{OFF}= 5 X 10^4

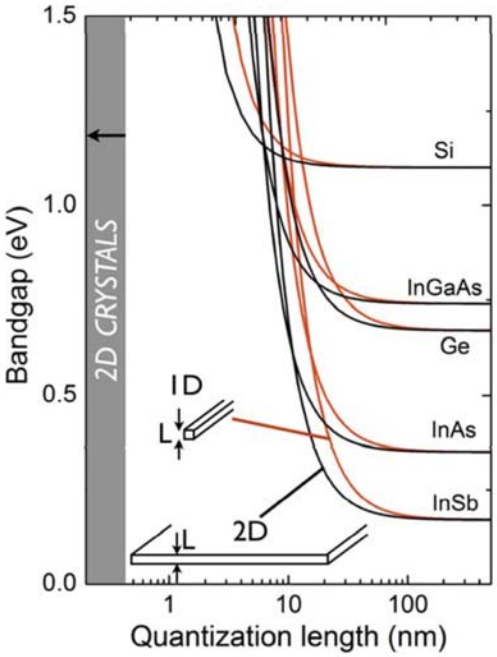
G. Zhou et al., *IEDM* 2012

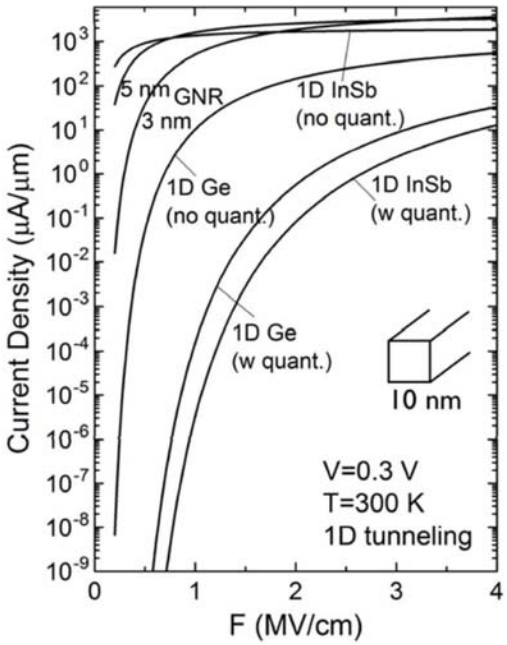
Culprit for poor SS



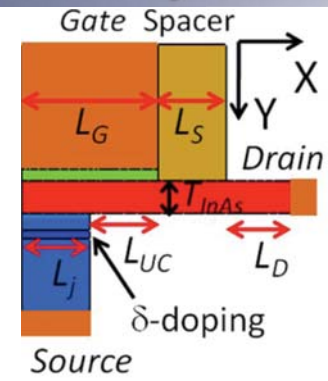
- **Poor D_{it}: > 1E14 / eVcm² near the conduction band edge by conductance method. High *SS* in InAs/GaSb TFETs.**

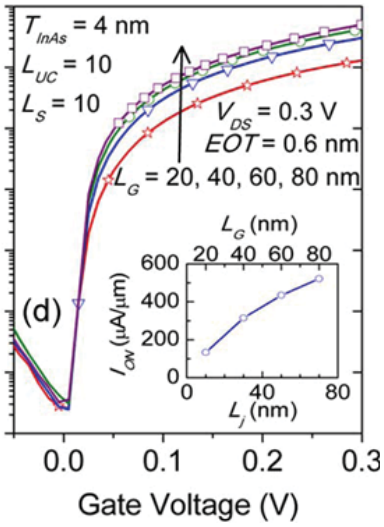
III-V and 2D-semiconductor TFETs: scalability





D. Jena, Proceedings of IEEE (2013)

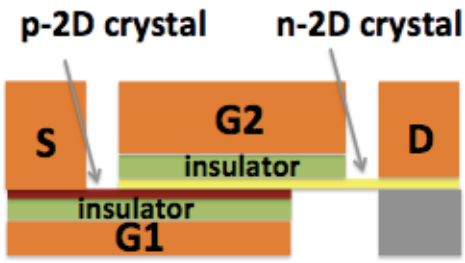




Lu et al, DRC (2011) & EDL (2012)

- Quantization renders sub-2 nm region inaccessible for 3D semiconductor TFETs
- Stacked TFET geometry offers unique electrostatic control of broken gap heterojunctions

Proposed approach in the LEAST center (Xing)



Why should it work?

- Operation in III-V TFETs has been proved.
- A variety of 2D crystals are available for desired band alignment.
- FETs have been already demonstrated in several 2D semiconductors.
- Out-of-plane transport has been demonstrated.

Statement of Work

- Investigate carrier control and transport as well as energy band lineup in 2D dichalcogenides together with other co-PIs in Theme 1-3, especially the effect of strain on the band structure of these 2D crystals.
- Model vertically stacked n-n and p-n junctions made of homo- and hetero- 2D dichalcogenides based on the outcome of the above task.
- Demonstrate experimentally vertically stacked p-n junctions made of 2D dichalcogenides.
- Understand out-of-plane tunneling transport between two 2D dichalcogenide layers and its dependence on doping, strain, relative crystallographic orientation, and layer thickness.
- Demonstrate tunnel FETs based on stacked 2D crystals.

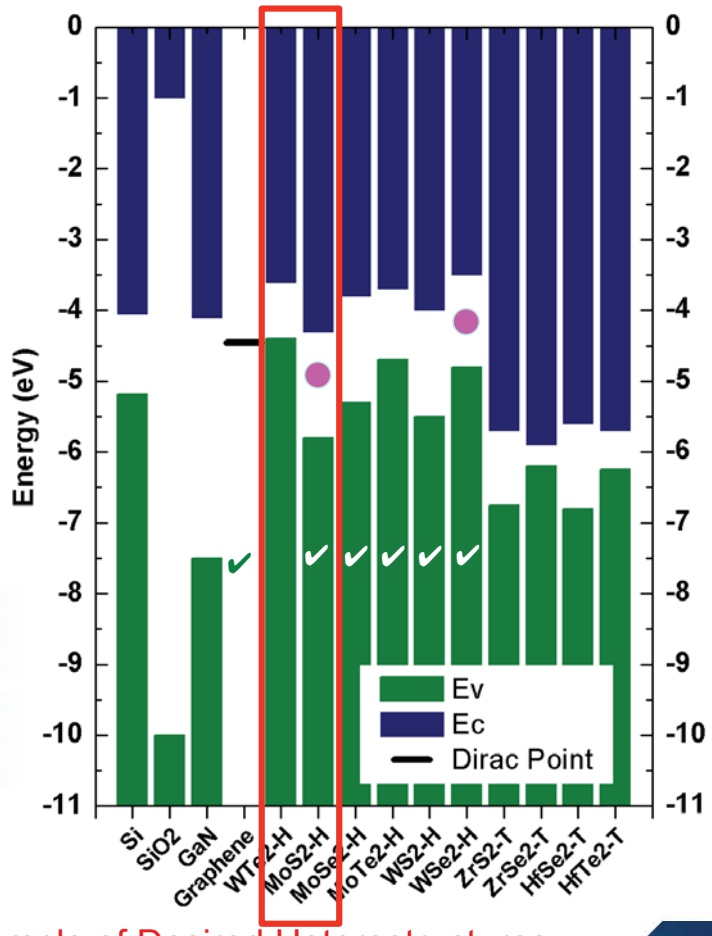
Near Term Goals

1. Apparatus set up to measure **energy band lineup** between MoS_2 and Si, MoS_2 and BN using internal photoemission (IPE)
2. Investigation on the **effect of strain** on the MoS_2 bandgap
3. I-V characteristics of **vertical stacked junctions**

● Vertical p-n junction demonstrated to date: n-MoS_2/p-WSe_2 (to be published)

✔ Back gated FETs demonstrated to date at ND

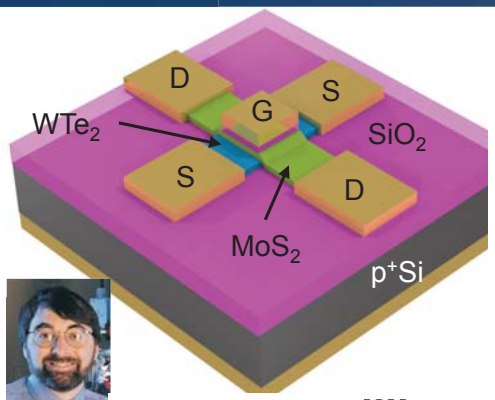
Monolayer TMD data from KJ Cho



Example of Desired Heterostructures

Stacked 2D TFETs: theory

Mingda Oscar Li (50% supported by LEAST)

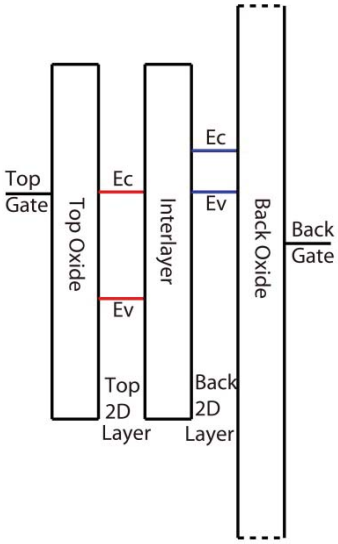


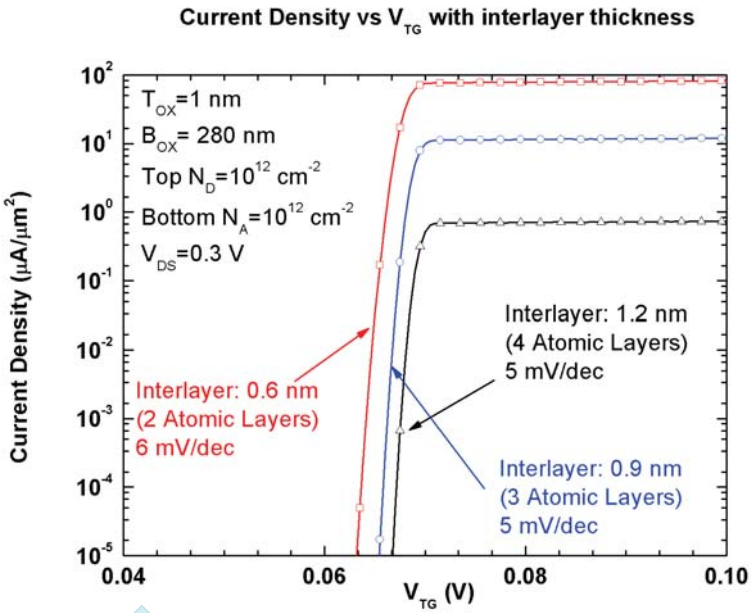
David Esseni

Greg Snider

MoS_2:
E_g=1.8 eV,
χ_e=4.3 eV
WTe_2:
E_g=0.7 eV,
χ_e=3.6 eV

Flatband energy Diagram





- **1D Poisson simulations (Snider)**
- **Bardeen transport Hamiltonian method (Feenstra, Jena)**
- **Tight binding**

- A single particle transport model has been developed; publication in preparation
- Calculated current density agrees well with what was published by the Manchester group

Mingda Oscar Li et al. To appear in JAP. arXiv: 1312.2557

Growth of MX_2 by MBE at UND (Unpublished)

Vishwanath
(50% supported by LEAST)

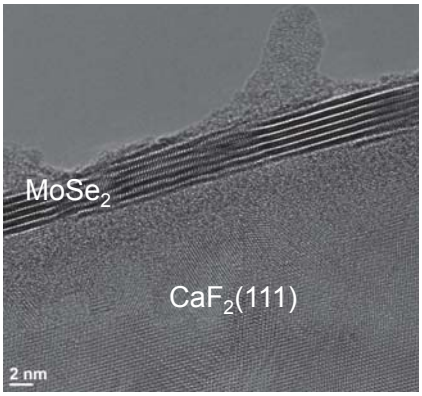
DJ

Prof. Xinyu Liu (UND, not LEAST researcher)

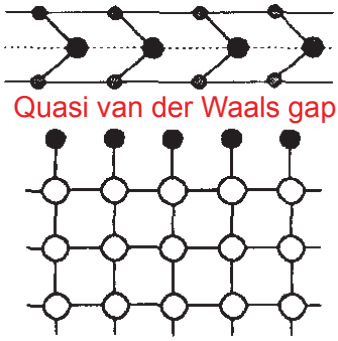
Goals
1. Layer controllable growth of (Mo,W)Se_2 and (Mo,W)Te_2 etc. by MBE.
2. MBE growth of h-BN.

Achievements
1. Few-layer $MoSe_2$ $SnSe_2$, Bi_2Se_3 grown by MBE, confirmed by TEM, EDS, Raman, RHEED, XPS, absorption spectrum.
2. Started h-BN growth.

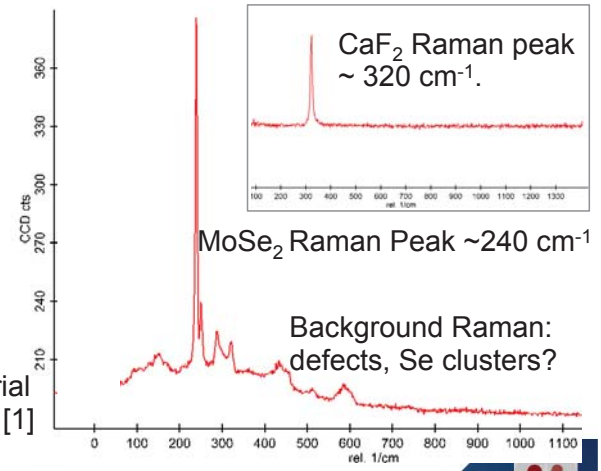
Plans
1. Optimization of growth.
2. Growth of vertically stacked heterostructures
3. Characterization of structural, electronic and optical properties



TEM of few layer (6-7) $MoSe_2$

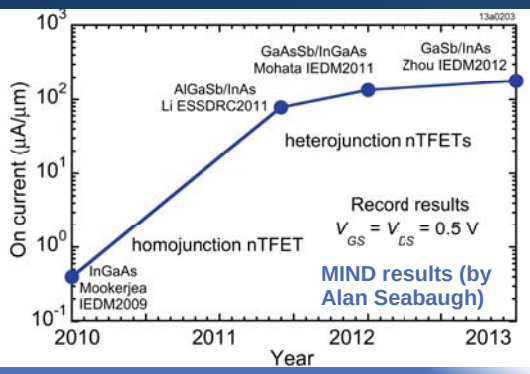


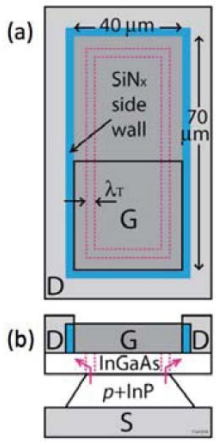
van der Waals epitaxy of 2D material on surface terminated 3D material [1]



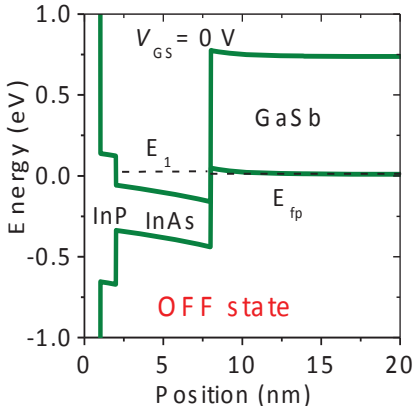
[1] Thin Solid Films, 216 (1992) 72-76

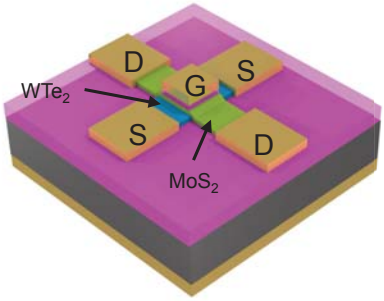
Steep transistors based on tunneling in compound semiconductors



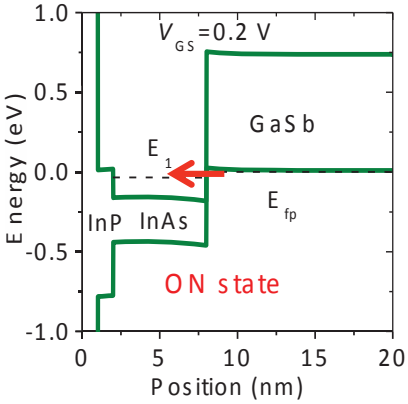


G. Zhou et al, EDL 2011





M. Li et al. JAP 2014. arXiv: 1312.2557



G. Zhou et al, IEDM 2012

III-V Tunnel FETs

- First demo of homojunction TFETs:
  Datta et al, 2009 IEDM
- First demos of Type-I TFETs:
  Xing et al, 2011 EDL
- First demos of Type-II TFETs:
  Datta et al, 2011 APEX;
  Xing et al, 2011 DRC
- First demos of Type-III TFETs:
  Wernersson et al, 2012 DRC
  Xing et al, 2012 IEDM

- Tunneling from quasi-3D source to 2D channel produces steep slope
- Near broken gap alignment produces steeper slope

Group and funding sources

Group Photo with
Dr. D. Jena's group

NSF: National Science Foundation
SRC: Semiconductor Research Corporation
NRI: Nanoelectronics Research Initiative
NIST: National Institute of Standards and Technology
DARPA. ARPA-E, ONR, AFOSR etc.