2.5 GB/s Germanium Gate PhotoMOSFET Integrated to Silicon Photonics

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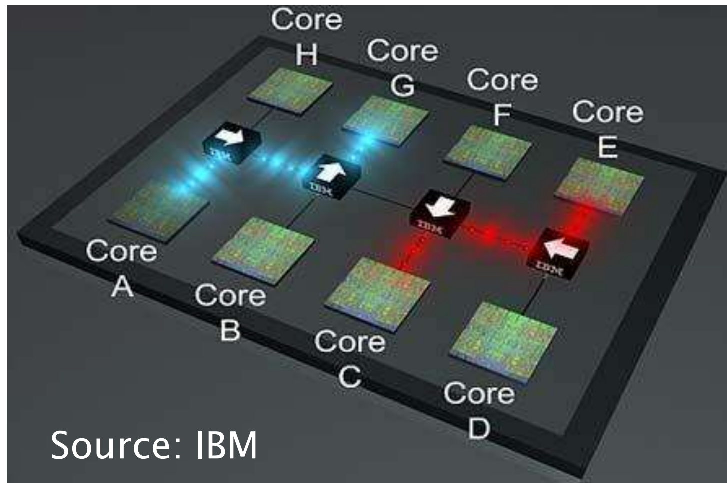
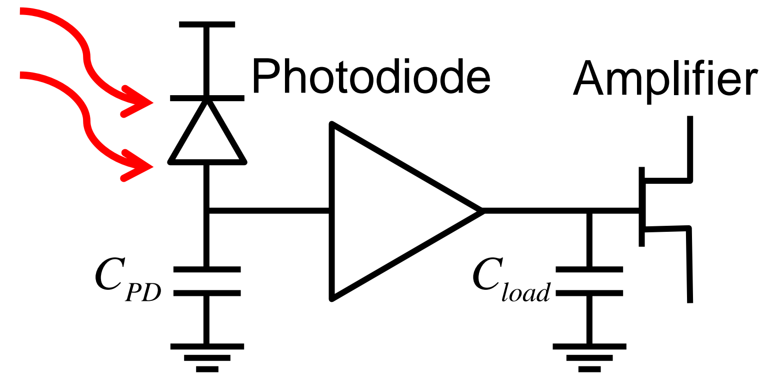
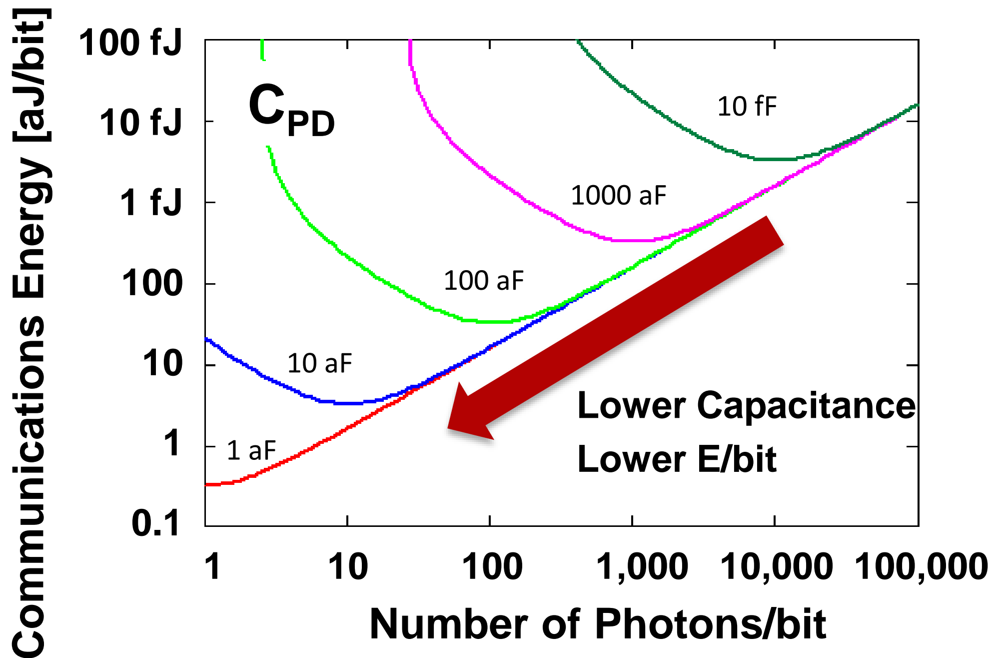
Why do we need an integrated transistor?





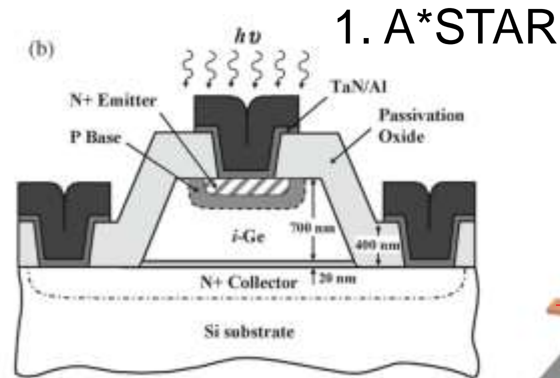


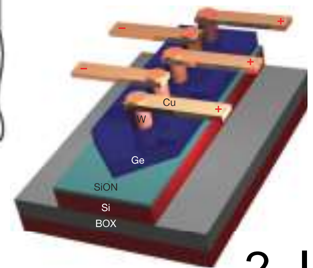
- **Need low energy receiver for future optical interconnects**
- **1 fJ/bit or less for receiver**
- **Reduce capacitance for low energy/bit receiver**
- **Wire from photodiode to transistor is 0.2 fF/μm**

Germanium devices with gain

1. **Bipolar Transistor**
   - **Bulk Si**
2. **Avalanche PD**
   - **SOI, waveguide**
3. **JFET**
   - **SOI, waveguide**
4. **poly-Ge gate FET**
   - **Bulk Si**
5. **c-Ge gate FET**
   - **SOI, waveguide**

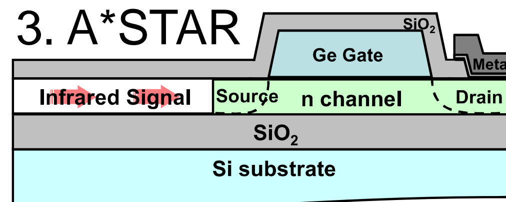
1. A*STAR



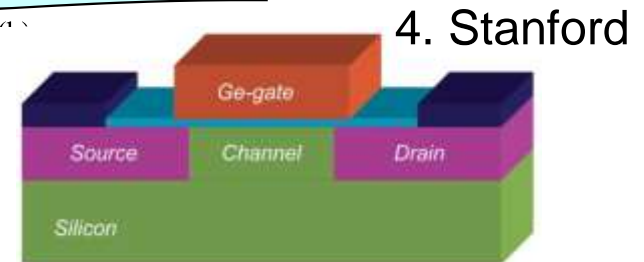


2. IBM

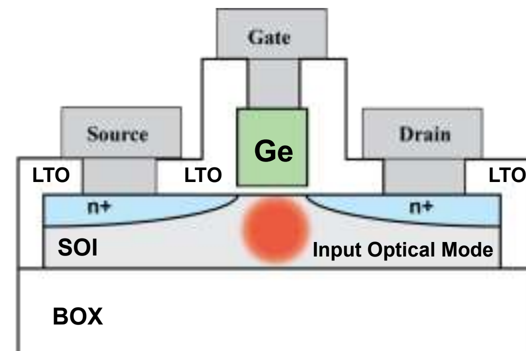
3. A*STAR



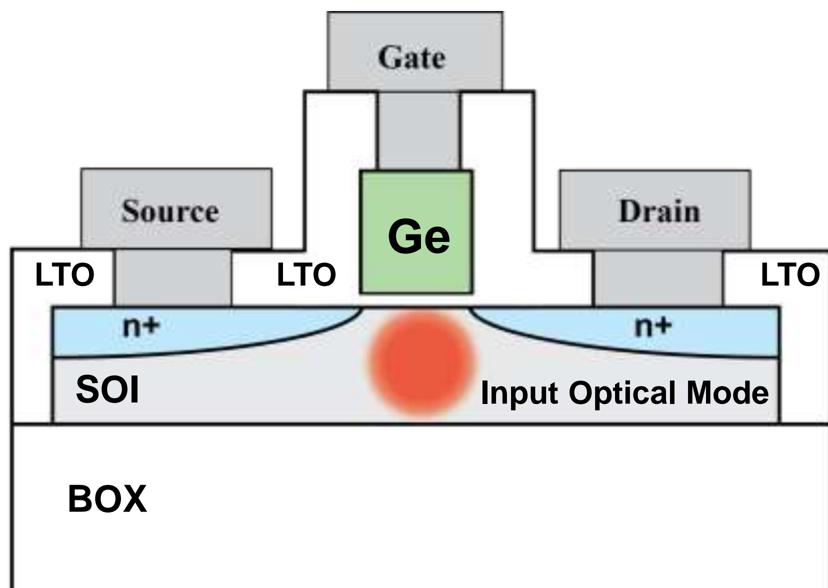
4. Stanford

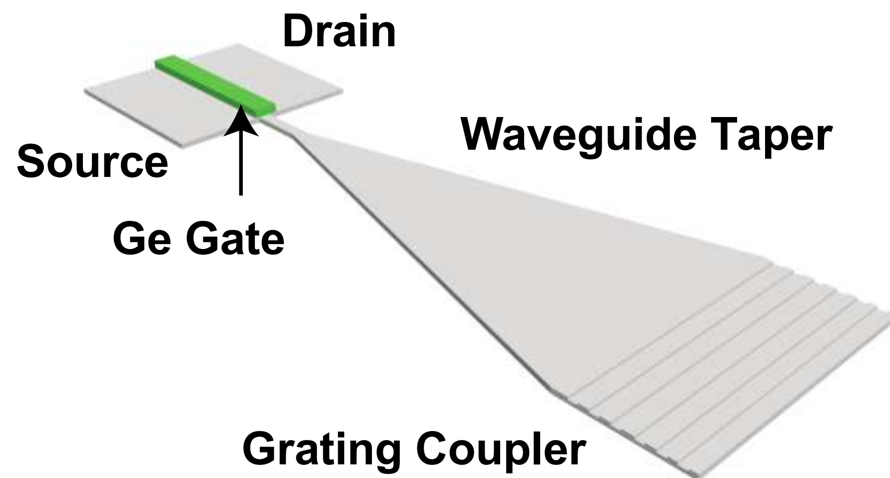


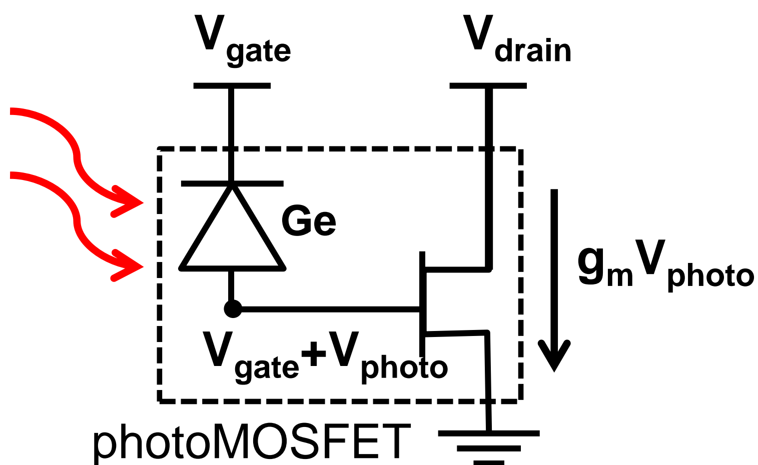
5. Berkeley



Device Design

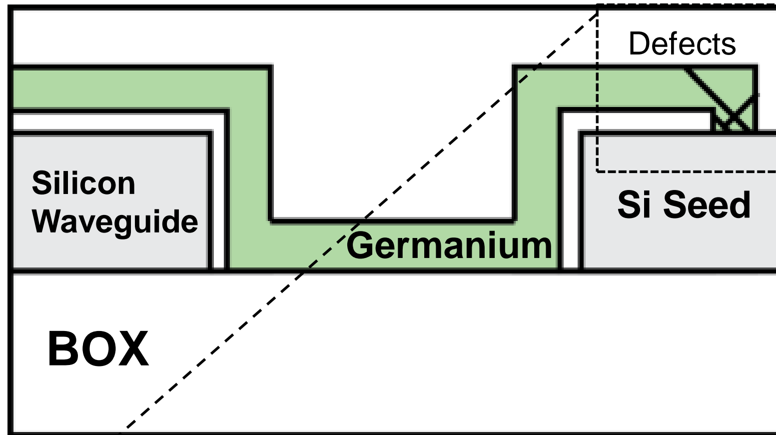


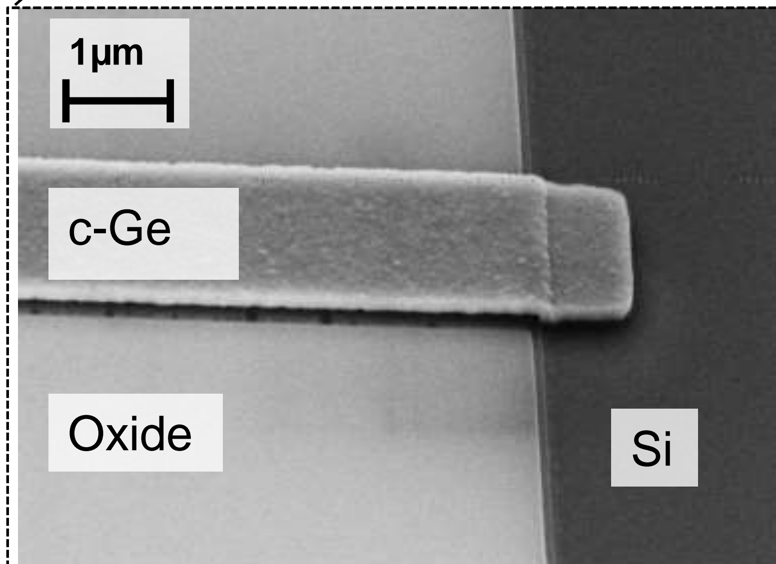




- **c-Ge gate SOI NMOS built on silicon photonics**
- **Evanescent waveguide coupling complements gate geometry**
- **Ge gate is an open circuit photodiode**
- **Gain mechanism: field effect transistor controlled by photovoltage**

Rapid Melt Growth



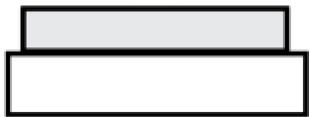


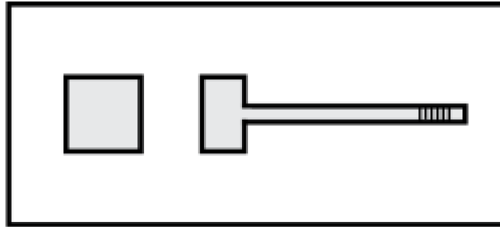
- Reported in 2005[1]
- Deposit Ge by CVD, sputtering, or evaporation
- Allows crystalline Ge on thin oxides
- Melt Ge at 1000°C for ~1s
- Defects terminate near silicon seed
- Low defect density (<10^6 cm^{-2})

[1]Liu, Y., Deal, M., and Plummer, J., J Electrochem Soc 152, G688–G693 (2005).

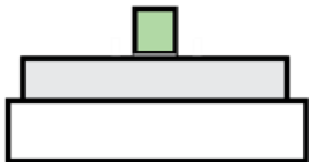
Fabrication of the photoMOSFET

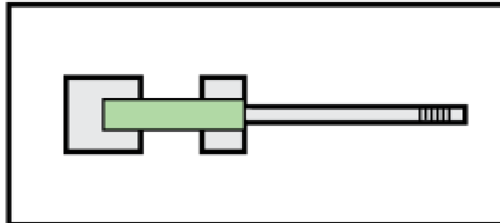
Si Photonics



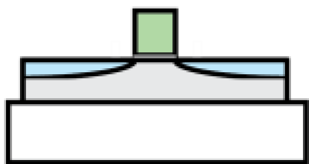


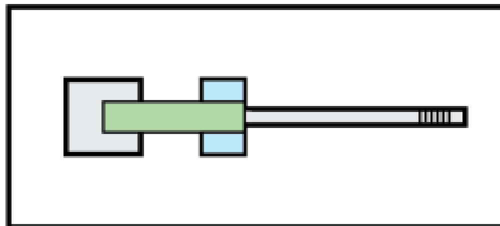
Gate Oxide, Ge deposit



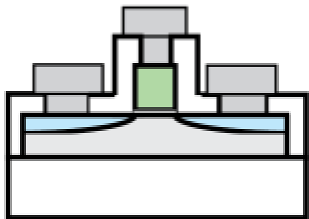


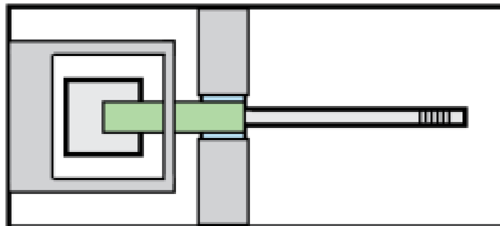
S/D Implant, RMG

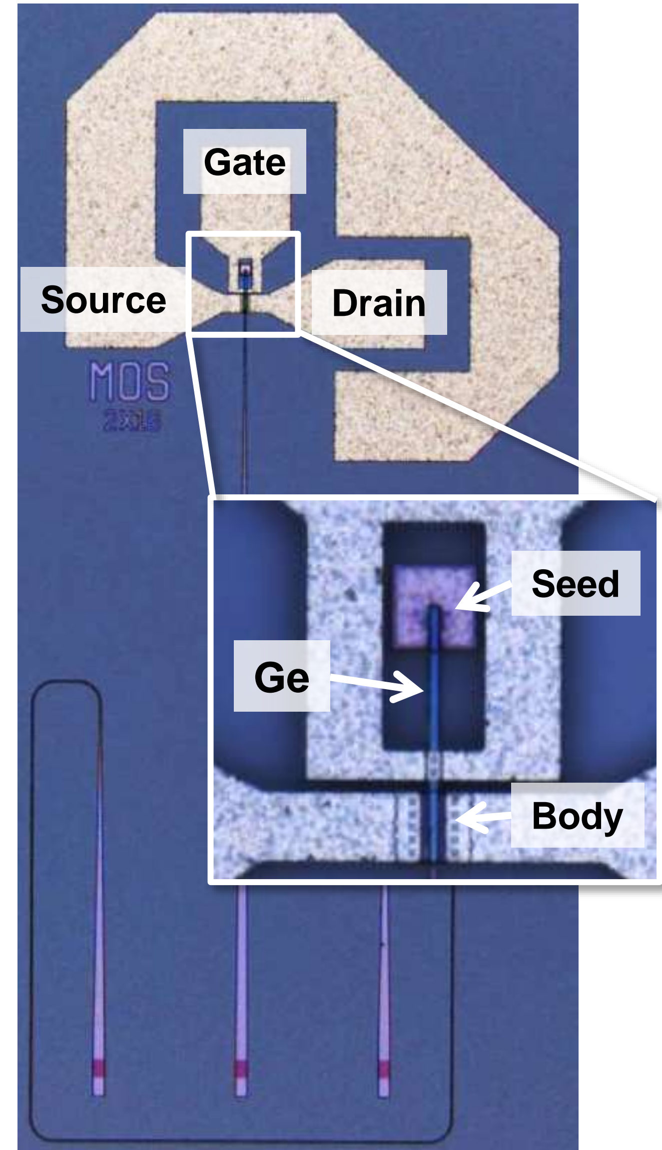




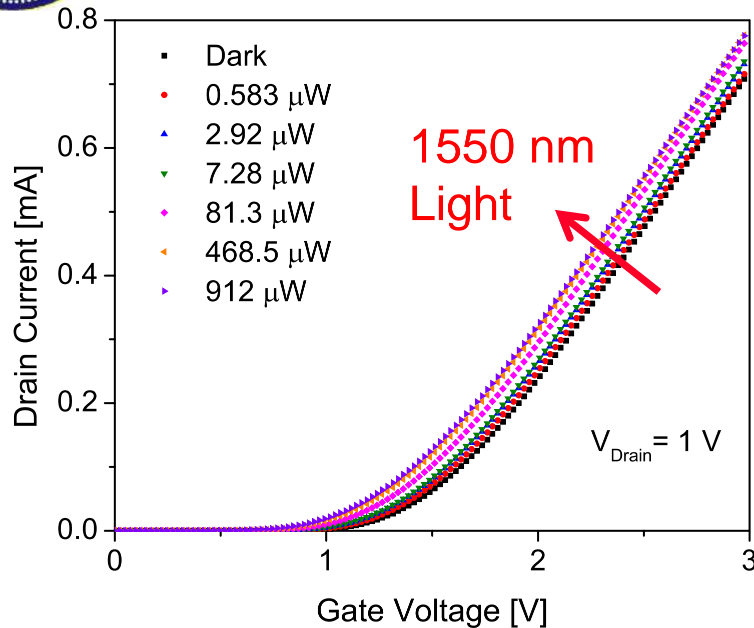
Metal Contacts

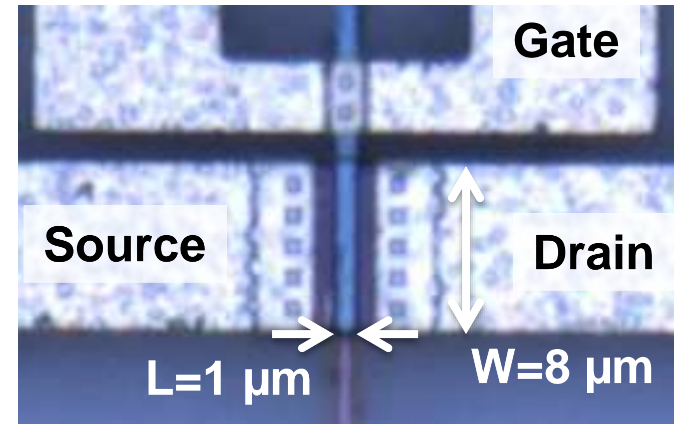


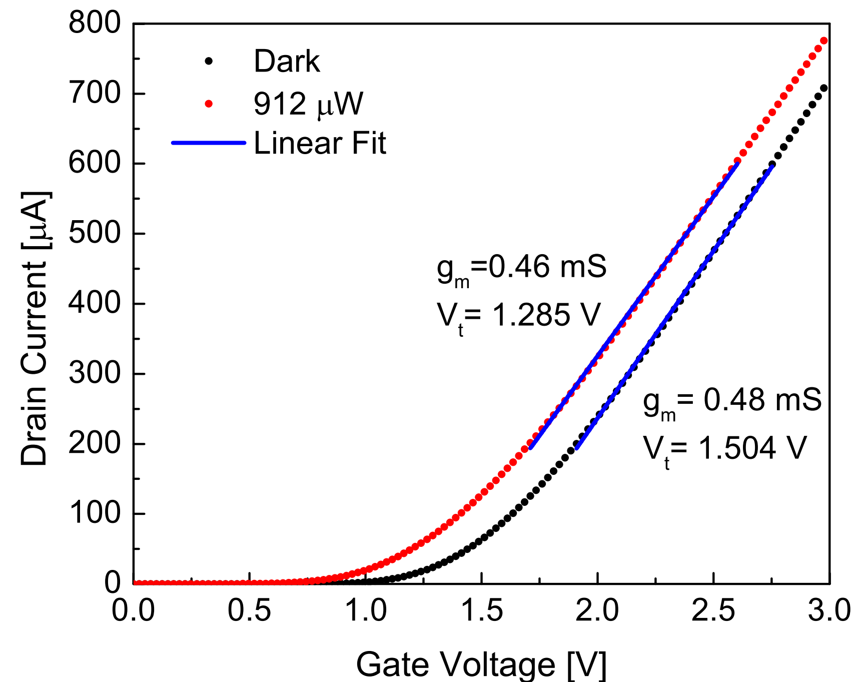




Voltage Shift with 1550 nm Light

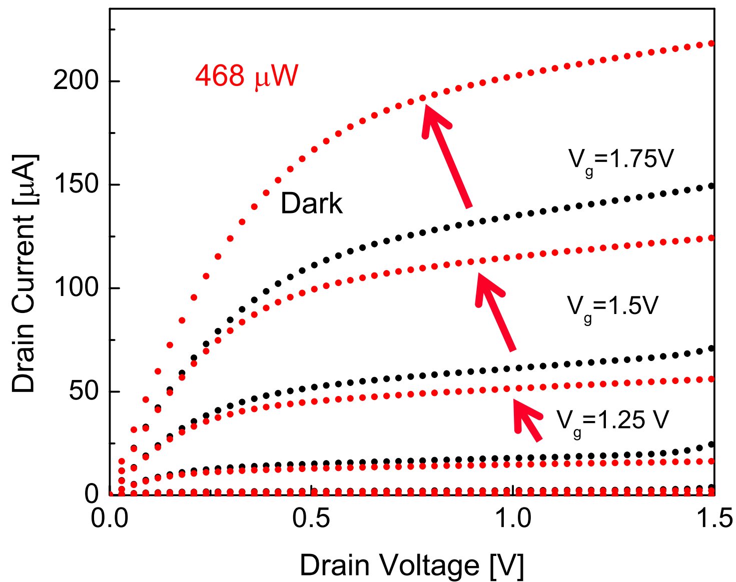




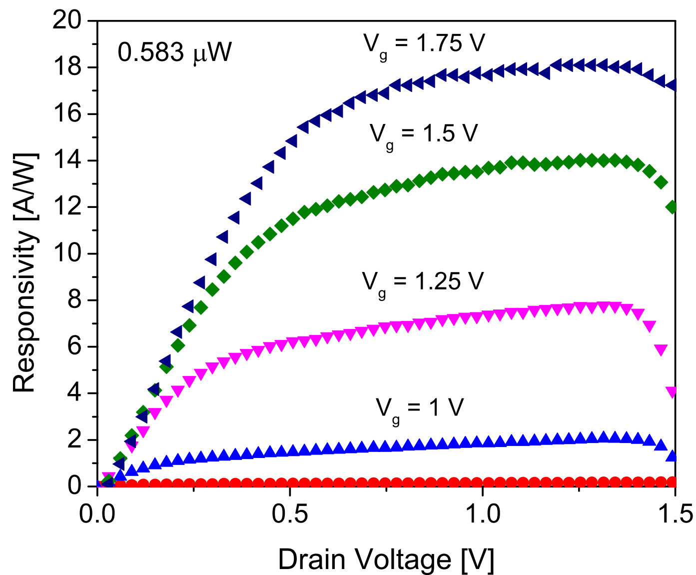


- **Excite with 1550 nm fiber probe through grating coupler**
- **g_m=60 mS/mm**
- **Measure voltage shift from linear V_T extraction**

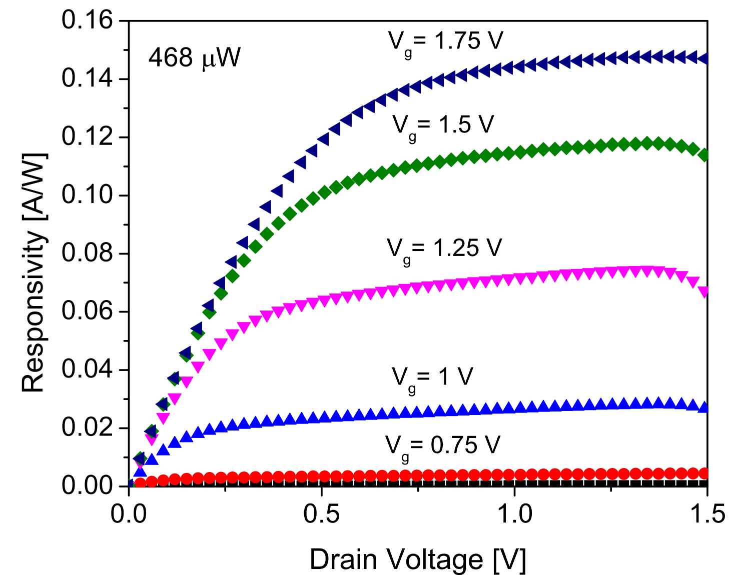
Bias Dependent Photocurrent



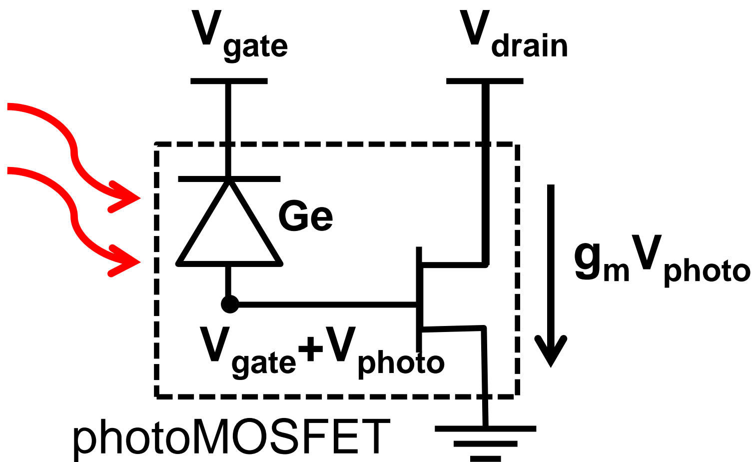
- **Larger bias current ➔ Larger gain**
- **Strong optical bias reduces gain**
- **Ability to bias electrically or optically**



+30 dB P_{inc}



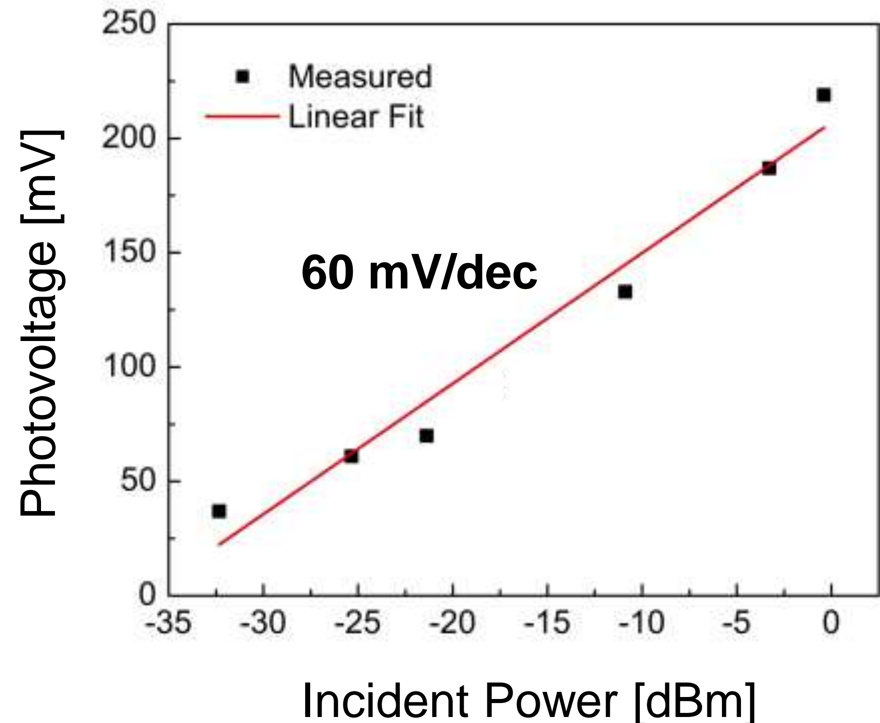
Photovoltage Revisited



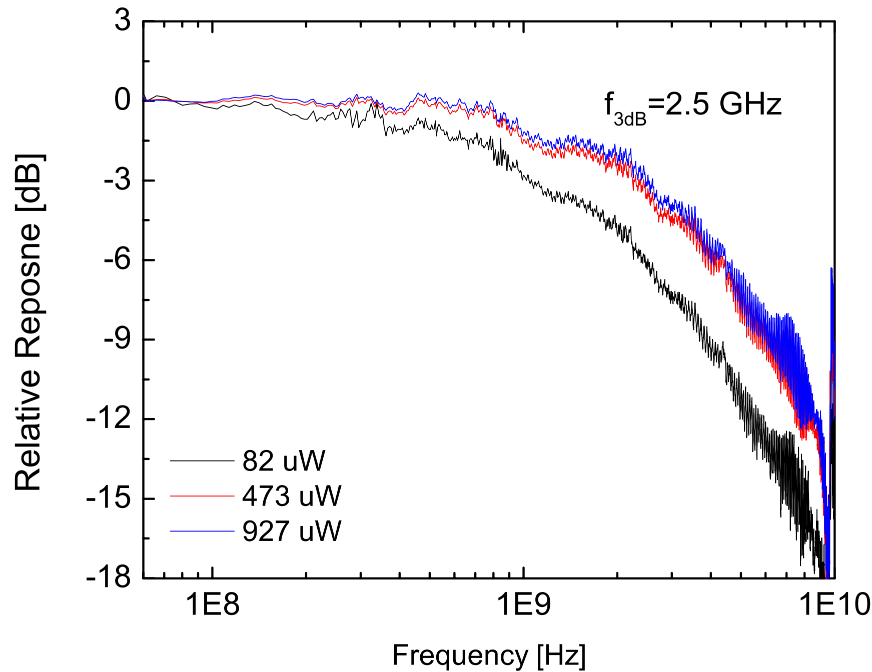
$$I_s\left(e^{\frac{qV_{photo}}{nkT}} - 1\right) = \eta \frac{q}{hf} P_{inc}$$

$$V_{photo} = \frac{kT}{q} \ln(P_{inc}) + const.$$

- **Photovoltage slope set by thermal limit (kT/q)**
- **Can be shifted by altering geometry, crystal quality (e.g. change I_s)**



High Speed Response

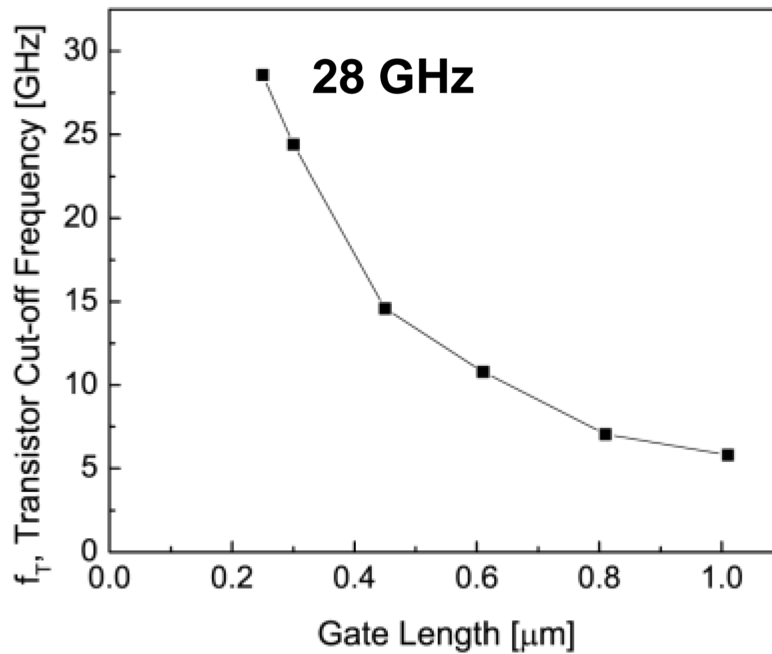


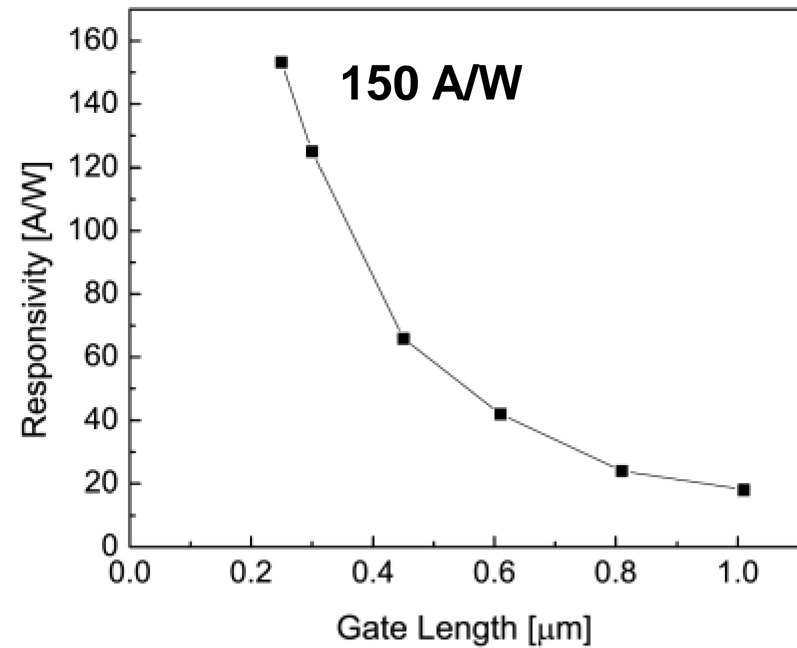
- **1x8 µm MOS, C_{ox}=20 fF**
- **Ge seed connected, C_{par}~5fF**
- **Use different optical biases to map gain x bandwidth product**
- **Device appears to be transit limited**

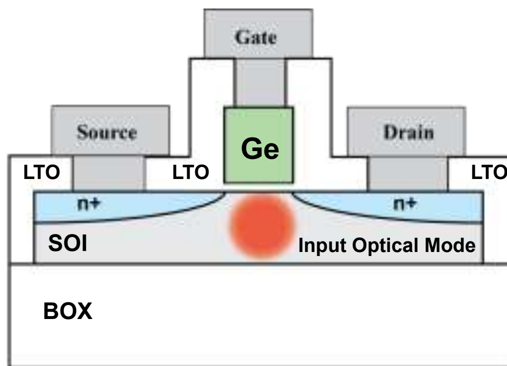
P_{inc} [µW]	Resp. [A/W]	Bandwidth [GHz]	Gain x Bandwidth [GHz]
82	0.698	1.5	1.05
473	0.164	2.4	0.39
927	0.0934	2.5	0.23

$$f_T = \frac{g_m}{2\rho(C_{ox} + C_{par})} = 2.9GHz$$

Simulation of gate scaling







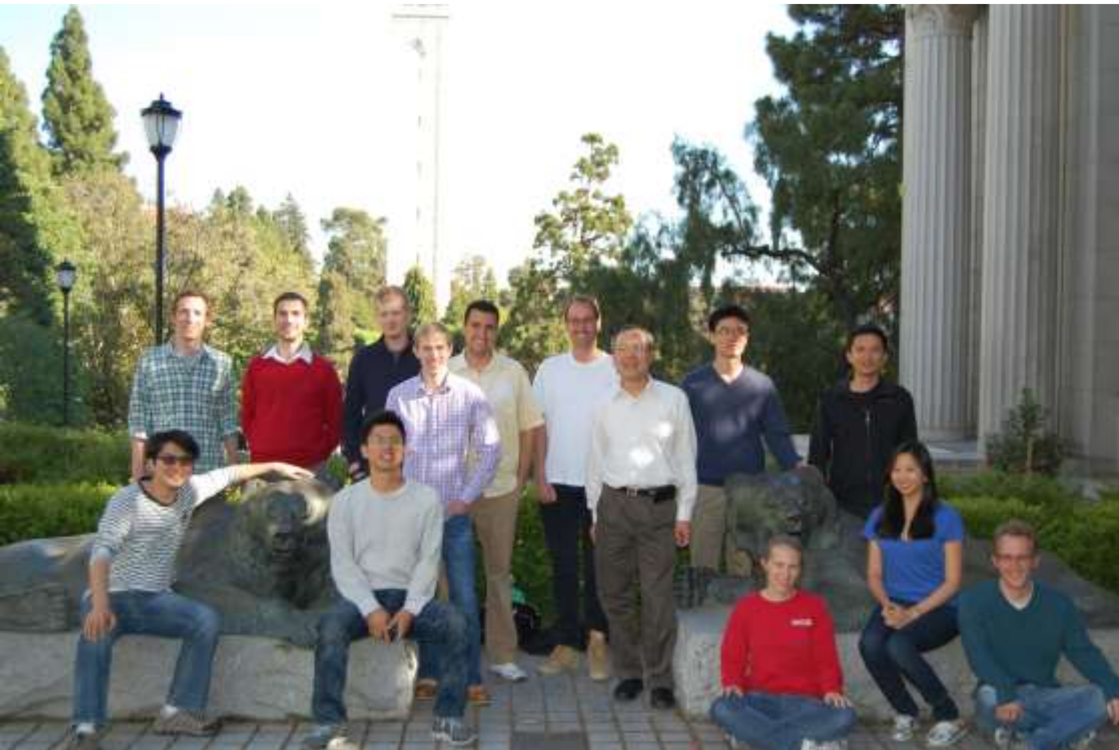
Gate Length, ↓
Gate Oxide, ↓
Junction Depth, ↓
Body Doping, ↑

- **Start with 1μm with our process**
- **Simulate constant field scaling**
- **Improvement in speed, responsivity**

Conclusions

- **Integrated crystalline Ge gate photoMOSFET**
  - **1 μm Channel length**
  - **R=18 A/W at 583 nW**
  - **f_{3dB}=2.5 GHz at 468 μW**
- **Standard scaling will improve performance**
  - **250 nm gate simulated with 28 GHz transit time, 150 A/W responsivity**
  - **Still room for optimizing implant profiles, oxide thickness, contact resistance**

Acknowledgments



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