NW-NEMFET: Steep Subthreshold Nanowire Nanoelectromechanical Field-Effect Transistor

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MOSFET Static Power Exponentially Dependent on S.S.

\[ P = ACV^2f + VL_{\text{leak}} \]

Dynamic

Static

\[ I_{\text{leak}} = I_G + I_{\text{GIDL}} + I_{\text{off}} \]

\[ I_{\text{off}} \propto \exp\left(\frac{-qV_{th}}{k_BT}\right) \]

\[ SS = \left| \frac{\delta V_g}{\delta \log I_d} \right| = \ln 10 \times \frac{k_BT}{q} \]

\[ P_{\text{static}} \propto V_{DD}I_{\text{off}} \propto \exp\left(\frac{-V_{th}}{SS}\right) \]
MOSFET S.S. are thermally limited by non-scaling factor $k_B T$
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- Abrupt electromechanical pull-in does not depend on $k_B T$
- Similar source-drain current as MOS when on

Input $V_g$

Output $I$

• PMOS
  - $I_{on}$
  - $V_{threshold}$
  - $V_{dd}$
  - $I_{off}$

• A ideal switch
  - $I_{on}$
  - 0
  - S.S.
  - $I_{off}$

UCSD Jacobs
Early Proposed NEMFET/Suspended Gate FET

Tsu-Jae, King et.al. IEDM (2005) 463-466.

Limitations of experimental suspended-gate FET

- Large gate mass limits resonant frequency to $\sim 16$ MHz
- High voltage and large on-off $V_g$ window $\sim 5$ V
- How does it scale towards NEMS?
What is “Nanoelectromechanical Systems (NEMS)”?
Nanowire Nanoelectromechanical Systems (NEMS) with GHz resonance

- Fast $f_0 \sim$ GHz
- Sensitive transducers
- Mass sensitivity: yocto~zepto gram
- Force sensitivity $\sim$ pN

Huang XMH, et.al., *Nature* **421** 496 2003 (Caltech)
NEMFET is not the following

2 / 3 Terminal NEM contact switches


- NEMFET does not require metal-metal or metal-semiconductor contact
- Potential to alleviate reliability concerns
NW NEMFET: Basic Device Design and Simulation

**Zero \(V_G\):**
- Nanowire
- Gate oxide
- Gate
- Source
- Drain

**Increase \(V_G\):**
- Mechanical force
- Electro-static force

**Pull-In Occurs:**
- Depleted

**Parameters:**
- \(W = 20\) (nm)
- \(L = 1300\) (nm)
- \(t_a = 2\) (nm)
- \(N_d = 1 \times 10^4\) (cm\(^{-2}\))
- \(V_{FB} (p^+\text{-poly gate}) = 0.0898\) (V)
- \(\varepsilon_{re}=\varepsilon_0=8.85 \times 10^{-12}\) (F/m)
- \(\varepsilon_a = 11.7 \varepsilon_0\)
- \(\varepsilon_{sa} = 3.9 \varepsilon_0\)
- \(\psi_b = 0.4702\) (eV)
- \(\mu_p = 500\) (cm\(^2\)/V-s)
- \(\mu_n = 204\) (cm\(^2\)/V-s)
- \(V_a (\text{w/o gap}) = 0.584271\) (V)
- \(V_a (\text{w/10nm air gap}) = 4.20009\) (V)
- \(V_a = -0.2\) (V)
Modeling NEMFET device characteristics

- $10^{15}$ on-off ratio within a 0.5V $V_{DD}$ window

- High $I_{ON}/I_{OFF}$ ratio within 1V $V_{DD}$ compared to 4V $V_{DD}$

- Higher p-doping of the NW leads to high off-current for the stuck-state
Gen 1 NEMFET: a contact switch

Process Flow

JH. Kim DRC (2013)
Gen 2 NEMFET: back gated

NW diameter : 28nm 
L_CH :
1.68um  
t_GAP  80nm Gate oxide 
40nm ZrO

V_PI : 10.8V  
V_PO : 6.5V  
I_ON/I_OFF : 10.7
S.S. : <15mV

JH. Kim DRC (2013)
Final NEMFET with HfO$_2$ dielectrics

Atomic level control of air gap reduction by ALD coating
Near Zero S.S. at Room Temperature

$V_{pi} - V_{po} = 1.6$ V

$V_{pi} : 14.48$V  S.S. : 6 mV/dec (limited by bin size)

$I_{on}/I_{off} : 2200$ (limited by stuck-state off current)

$I_{on} = 2 \mu$A
Stable, multiple switching with $< 1$V voltage window

- Initial rise but stabilized operational voltage window $(V_{pi} - V_{po}) = 0.83 \pm 0.52$ V
- Eventually failed due to stiction.

JH. Kim (submitted)
NEMFET resonance at 126 MHz (VHF)

\[ I = G V_{sd} = (G^{DC} + \tilde{G}^{\omega})(V_{sd}^{\omega+\Delta\omega}) \]

\[ = G^{DC} V_{sd}^{\omega+\Delta\omega} + \tilde{G}^{\omega} V_{sd}^{\omega+\Delta\omega} \]

\[ I^{\Delta\omega} = \frac{1}{2} \frac{dG}{dq} \left( C_{g}^{\prime} \omega(\omega)V_{g}^{DC} + C_{g} V_{g} \right) V_{sd} \]

\[ V_{d}^{ac} = 140mV \]

\[ V_{d} = 120mV \]

\[ V_{d} = 100mV \]

\[ V_{d} = 80mV \]

\[ V_{d} = 60mV \]

\[ V_{d} = 40mV \]

\[ I_{\text{MIX}} \] measurement with 400Hz/99% AM modulation

Measured \( f_0 = 126 \text{MHz}; Q = 630 \) at 40 mV drive.

Quadratic dependency of \( f_0 \) to AC drive voltage
Gate and bias dependence of resonance frequency elucidates how nanowire is tensioned and driven

- $f_0$ vs. $V_g$

  → Elastic Hardening. Nanowire has no slack

- $f_0$ vs. $V_d$

  → Capacitive Softening (Effective side gate effect)

JH. Kim (submitted)
Device Speed and Scaling – a design window for Si-based NW NEMFET

- Airgap fixed at 10 nm.
- >300 MHz with 5 V $V_{\text{pull-in}}$ can be achieved using SiNWs with 11.7 nm diameter. Readily available in our laboratory.
- Sub 1V operation for diameter smaller than 5 nm.
- More aggressive scaling with CNT, graphene and other 2D monolayer materials.
Conclusion

Low-Power, High-Speed NEMFET

- ~ 0 mV/dec S.S. circumvents thermodynamic limit to sharp switching
- VHF operation with small voltage window requirements (< 1 V) due to nanowire beam structure
- Can enable both logic and non-volatile memory

Next steps:
- Improvements needed on doping and surface states control in Si/Ge based channels.
- Further scaling and interface fixed charge planting for reduced $V_{pi}$. Explore new carbon-based or molecular monolayer materials.