Silicon Carbide Nanoelectromechanical Systems (SiC NEMS)
→ Logic for Energy Efficiency, Longevity & Extreme Conditions

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E3S Symposium | Berkeley, CA | October 28-29, 2013
Very Bright Students!

Private, Small, Integrated, High Quality

... Case Tech (aka, CIT-style ‘nerdy’ culture)

... very high Faculty-Student ratio

Excellent Academic Reputation

... a good number (~16) of Nobel Prize Laureates

... including the 1st US Physics Nobel Prize

Top-Ranking Medical School and Hospitals

Outstanding Records in High-Tech Start-Ups

... many technology inventions (e.g., walkie-talkie)

... many entrepreneurial activities (e.g., Dow)
Great Legacy & New Excitement at Case EECS for Devices/Systems

- A leading institute in MEMS, Microsystems and Solid State Transducers
- A pioneering program in BioMEMS, Bio-Implanted Devices/Systems
- Excellent programs in Advanced Materials, Microelectronic Circuits & Systems

Case Channel on Youtube:  http://www.youtube.com/user/case
Advancing *High-Speed ‘Nanomachines’* → New Devices

- **Atomically-Thin 2D Crystals → Sensing**
  - Exploring Multiphysics Coupling in ‘Meso’ Systems
  - Ideal Platforms for Flexible & Stretchable Devices
  - Single-Molecule Nano-Bio-Sensing
  - New Probing Techniques for Surface Sciences

- **NEMS RF Signal Processing**
  - Use NEMS/NEMS to Tune Electronics
  - Active & Coupled Oscillators (Timing, Sync)
  - RF Filters, Mixers, Amplifiers, *etc.*
  - Exploring New Dynamics in ‘Meso’ Systems

- **Ultralow-Power Logic & Computing ↔ ‘Steep-Slope’ Devices**
  - No Leakage, High On/Off Ratio
  - → Power Hungry + Harsh Environment
  - → Quest for the Ultimate Switching Devices
The Power Crisis & Bottleneck – A LOT of HEAT

Chip/Module Power Density Scaling

Nowark, IBM, 2002
Crisis Origins at the **Device Level** – **Standby Power Crisis**

**Leakage !!**  
\[ V_G = 0 \text{ V} \]
\[ V_D = 1.2 \text{ V} \]

\[ V_B = 0 \text{ V} \]

Need Steep Subthreshold Slope Switches!!
Static Power Crisis: Thermally-Limited Subthreshold Slope

\[ P_{\text{static}} = V_{DD} \cdot N \cdot I_{\text{leak}} \]
\[ I_{\text{leak}} = I \bigg|_{V_g=0} \]
\[ = I \bigg|_{V_g=V_T} \cdot \exp\left(-\frac{qV_T}{k_BT}\right) \]
\[ = I \bigg|_{V_g=V_T} \cdot \exp\left(-\frac{V_T}{S}\right) \]
\[ S = \frac{2.3k_BT}{q} = 60\text{mV/dec}(300K) \]

- \( V_T \) not well scaled, facing multiple limitations as \( \rightarrow 0.2\sim0.4 \text{ V} \)
- Ways of lowering \( S \) is key to ‘beat the system’ (\( i.e., S<60 \text{ mV/dec} \))
- New switch mechanisms to replace or amplify Sub-\( V_T \) nonlinearity
- Need Steep Subthreshold Slope Devices (SSS FET) – Possibilities
  - Impact Ionization; Inter-Band Tunneling, Mechanical Motion
Hybrid Devices $\rightarrow$ Suspended Gate/Channel (‘SG/SC’) FET

- $V_{pi}$ within $V_{DD}$ of transistor
- $V_{pi}$ at weak inversion/accumulation region
- $V_{po} > 0$, suspended structure rigid enough
- Bandwidth consideration – Scaling to NEMS dimensions

Nanoelectromechanical Switches – Basic Ideas

- Actuation Schemes: Electrostatic, Piezoelectric
- Configurations (for each scheme): Lateral (In-Plane), Vertical (Out-of-Plane)
- Improve subthreshold slope/swing (could be with hysteresis)
NEMS’ Merits:
- No Leakage
- High ON/OFF
- Fast (High $f_0$)
- High-T OK
- Radiation OK
- Size Good (< MOSFET)
- Low Op. Power

Possibilities:
- All Mechanical
- Hybrid NEMS-CMOS
Nanoelectromechanical Devices & Systems (NEMS)

- Further miniaturization of today’s MEMS (to ~<100nm)
  - Mechanical degrees of freedom → Vibrating / Resonating (Q)
  - Design, fabricate & measure smallest possible

- **Bottom-Up** (Chem. Synthesis) vs. **Top-Down** (Lithography)

  ![Dispersing Au clusters to VLS growth of Si nanowires](image)

  Device Complexity (Multilayer, Arrays...)  
  More Room for Design Innovations, etc.

  Toward Molecular-Scale Devices, Pristine Surfaces, etc.
Team Caltech (2007 – 2010)

**PI:** Prof. Michael Roukes

**Co-PI / Staff Scientist (Technical Lead):** Dr. Philip Feng

**Graduate Student (Ph.D. Candidate, Applied Physics):**
Mr. Peter Hung

**Graduate Student (Ph.D. Candidate, Physics):**
Mr. Matt Matheny (Now Graduated)

**Staff Scientist:**
Dr. Rassul Karabalin
(Now at Tower Jazz)

**Kavli Fellow (2007):**
Dr. Jie Xiang
(Now Prof. at UCSD)

**2008-2010 SURF:**
Mr. Nick Scianmarello (Caltech EE), Matt Yu (Stanford EE)
Mr. Joshua Yoon (Stanford Physics)
Mr. Abraham Chien (Laserfiche), Derek Chou (Berkeley Physics/EE)
Very Thin (100nm, 70nm) SOI NEMS Switches

*Lateral (In-Plane) Electrostatic Devices*

Feng, *et al.*, US Patents #8,258,899, #8,115,344
Electrostatic NEMS with Simple **Lateral** Contact

- Generic prototype of electrostatic NEMS cantilever switch
- Compatible with both 2-terminal & 3-terminal operations

- use both *pull-in* and *pull-off* gates, Au metallization
- ~50–100nm electrostatic coupling gap ("gate")
- ~20–40nm switch gap ("source-drain")
- ~100% yield for large-scale patterning with hundreds of devices
- 1\textsuperscript{st} Gen. devices: \( f_0 \sim 1–10\text{MHz} \), switching speed \( t_s \sim 100–10\text{ns} \), typical \( V_{\text{on}} < 10\text{V} \)
Other NEMS Switch Prototypes with Lateral Contacts

- With lateral point contact and multiple gates (multifunctional)

- Dual-beam with multiple gates (multifunctional)

Feng, et al., US Patents #8,258,899, #8,115,344
Data: 3-Terminal Electrostatic NEMS Switches

- Thin SOI Devices (100nm Si on 400nm SiO$_2$) with Au-Au Contacts

- L=7µm, w=100nm, t=100nm, $g_{DS}$$\approx$30nm

- L=1µm, w=100nm, t=100nm, $g_{GS}$≈35nm, $g_{DS}$≈15nm

- L=9µm, w=100nm, t=100nm, $g_{GS}$≈60nm, $g_{DS}$≈30nm
Metallized SOI – Smallest Lateral Cantilevers

$L=700\text{nm}$, $w=100\text{nm}$, $t=100\text{nm}$
Coupling gate length=400nm
Coupling gap=70nm
Switching gap=15nm
Cantilever resonance = 213.7MHz

VLSI Patterning on SOI
(100nm Si on SiO$_2$)
via Leica (Vistek) EBPG 5000+

Anisotropic Etch of Si
HF Etch of SiO$_2$ (w/o CPD)

No Stiction after wet etch with these short devices
Towards Logic Gates with More Reliable Contacts...

- All-NEMS Inverters based on Very Thin (70nm) SOI
  *Left:* All-Si SOI devices

*Right:* All-Si SOI devices with metal leads
**In-Situ Measurement & Imaging of NEMS Switching**

**Inside SEM and Vacuum**

- Intimate understanding for the process when the device undergoes switching
- Pristine environment → approaching device’s intrinsic performance
- Lay foundation for future hybrid devices (to be in advanced packaging)
- Ideal for controlled experiments in contact physics and NEMS materials
Simply conductive Si, no metallization layer

![Device Images]

![IV Characteristics Graphs]
Quick Summary – Major Challenges

- Very Limited # of Cycles & “Lifetime” (Hot vs Cold Switching)
- Suffering: Large Majority of Today’s NEMS
- Nanoscale Contacts...
Introducing Silicon Carbide (SiC)

Why SiC?!
A Quick Recap on SiC & Harsh/Extreme Environments

Harsh or Extreme Environments

- High temperature (>350°C)
- High shock (>50,000g)
- High radiation (>100 MRads)
- Erosive flow/impact (abrasive particulates in flow, frictional bearing/contact)
- Corrosive media (oxidative, caustic, acidic)

Demanding

- Requiring intrinsic material properties beyond Silicon, for example higher: modulus, fracture toughness, acoustic velocity, thermal conductivity; surface inertness
SiC NEMS: Caltech-CWRU (2001-09) Technology Roadmap

- 3C-SiC, 80-100nm Mechanically-Coupled Beams
- 3C-SiC, 80-100nm Free-Free Beam
- 3C-SiC, 80-100nm Parametric Resonators
- Poly-SiC, 400-500nm Lateral NEMS Switches
- Poly-SiC, 400-500nm Lateral NEMS Switches
- 3C-SiC, 50nm Multifunctional NEMS
Two-Terminal SiC Nanowire Switches

Lithographically-defined SiC nanowires (with 50nm SiC on Si)

$L = 15\mu m$
$w = 55nm$
$t = 50nm$
$t_m = 30nm$

Case SiC NEMS Logic Team (Fall 2011 – Now)

Philip Feng
Assist. Prof.
EECS, Case

Swarup Bhunia
Assoc. Prof.
EECS, Case

Mehran Mehregany
Goodrich Professor
EECS, Case

Tina He
Graduate Research Assistant
Ph.D. Student in EE

Vaishnavi Ranganathan
Graduate Research Assistant
M.S./Ph.D. Student in EE

Rui Yang
Graduate Research Assistant
M.S./Ph.D. Student in EE

Hari Rajgopal
Research Associate
NEMS for Logic (SiC): Device Technology Roadmap (Tested)

- Nanoscale Switches
- Only Length ($L$) is Not Sub-Micron
- Very High Speed ($f_0 > 10 - 100$ MHz)
- Low Voltage ($V_{on} < 3-5V$)

Nano Letters (2010)
Science (2010)
DARPA MFG Workshop (2011)
IEEE MEMS (2013)
IEEE NEMS (2013)
IEEE IEDM (2013)
IEEE MEMS (2014)
SiC Lateral NEMS Switch Designs

- Designing with the trade-off between $V_{on}$ and $t_s$
- Various designs with dimensions swept in arrays of devices

Switch-On Voltage, $V_{on}$ (Volt)

Switching Time, $t_s$ (ns)

Single Die, Run 2 (2011)
4” & 6” Wafer-Scale Fabrication Processes

(a) 
(b) 
(c) 
(d) 
(e) 
(f) 
(g) 
(h) 
(i) 
(j) 
(k) 

Si  SiO₂  Poly-SiC  Au  PMMA  Ni
4” & 6” Wafer-Scale Fabrication Processes

- **New Release Process**
  - Vapor HF
  - Higher Yield

- **Wafer-Scale Electron-Beam Lithography (EBL)**
  - High Precision and Uniformity
  - High Yield
  - Yield Study: Bi-Layer Resist (Run 2/2010-2011) vs Mono-Layer (Run 3/2012 – currently in fab process)
SiC NEMS Logic Switches – *Basics*

Device Characteristics in Ambient Air (~300K)

He, Yang, Rajgopal, Tupta, Bhunia, Mehregany, Feng, *IEEE MEMS 2013*
He, Ranganathan, Yang, Rajgopal, Bhunia, Mehregany, Feng, *Transducers 2013*
He, Yang, Feng, *et al.*, *IEEE IEDM 2013*
Basic *I-V* Characteristics in DC Measurement – (1)

### *I-V* Characteristics

- Switch-On voltage, $V_{On}$
- Switch-Off voltage, $V_{Off}$
- On State Current/Resistance, $I_{ON}/R_{ON}$
- Off-State Current

**Basic I-V Characteristics in DC Measurement**

- Switch-On voltage, $V_{On}$
- Switch-Off voltage, $V_{Off}$
- On State Current/Resistance, $I_{ON}/R_{ON}$
- Off-State Current
Basic $I$-$V$ Characteristics in DC Measurement – (2)
Careful Calibration for Proper Operating Regime

- Real switch-on or threshold voltage: $V_{on}$
- $V_{PI,G}$ (cantilever vs clamped-supported beam)
- Range: $(V_{on}, V_{PI,G})$
- Practically, critically important in testing!
Basic $I$-$V$ Characteristics in DC Measurement – (3)

(a) $I_D$, $I_G$

(b) $I_D$, $I_G$

(c) $V_G$, $I_D$

(d) $V_G$, $I_D$

$I_{on} > 1\mu A$
Clear Control Expts – Subthreshold ($V_{G,pk} < V_{on}$) Actuation

**$V_{G,pk} > V_{on}$**

![Drain Current vs Time for $V_{G,pk} > V_{on}$](image1.png)

**$V_{G,pk} < V_{on}$**

![Drain Current vs Time for $V_{G,pk} < V_{on}$](image2.png)

**Gate Voltage vs Time for $V_{G,pk} > V_{on}$**

![Gate Voltage vs Time for $V_{G,pk} > V_{on}$](image3.png)

**Gate Voltage vs Time for $V_{G,pk} < V_{on}$**

![Gate Voltage vs Time for $V_{G,pk} < V_{on}$](image4.png)
SiC NEMS Logic Switches – *Performance*

Long Cycles Recorded in Ambient Air

He, Yang, Feng, et al., *IEEE MEMS 2013*
>14,000 cycles in 7 consecutive days

Still alive (now preserved in vacuum)
Zoom-In Details

Day 1, Box ① Segment

Day 7, Box ⑦ Segment

Drain Current, $I_D$ (A)

Gate Voltage, $V_G$ (V)

Time (s)
Checking the $I$-$V$ Characteristics

- **Day 1** ①
  - At Beginning

- **Day 7** ⑦
  - At the End of All Recorded Long Cycles

![Graphs showing I-V characteristics](image)

- **Current, $I_{DS}$ (A)**
  - $10^{-15}$
  - $10^{-13}$
  - $10^{-11}$
  - $10^{-9}$
  - $10^{-7}$

- **Gate Voltage, $V_G$ (V)**
  - 0 to 25

(a) Graph for Day 1
(b) Graph for Day 7
Brief Summary of Section

- All key information of the evolution recorded in real time.
- Careful and clear control experiments.
- Highly repeatable in multiple devices from same batch (some >10^6 recorded cycles).
- Current status: all preserved in vacuum (for future new testing).
SiC NEMS Logic Switches – *Performance*

AC Testing in Ambient Air

He, Yang, Feng, *et al.*, *Transducers* 2013
AC Measurement of Multiple Switching Cycles

Challenges

- $R_{ON}=1k\Omega \sim 10M\Omega$
- $I_{ON} < 1\mu A$

Instruments

“Probe-Up Calibration”

$V_{o}(V)$

$V_{o}(V)$

Gate Voltage, $V_G$ (V)

Time (s)

Output Voltage, $V_O$ (V)

Probe Station

Testing PCB
PSpice Simulation of the Testing Circuit Board

\[ R_{on}, R_b, C_p = \begin{cases} (b) \ 1\,\text{M} \Omega, 1\,\text{M} \Omega, 3\,\text{pF} ; \\ (c) \ 10\,\text{M} \Omega, 1\,\text{G} \Omega, 3\,\text{pF} ; \\ (d) \ 100\,\text{M} \Omega, 1\,\text{G} \Omega, 3\,\text{pF} \end{cases} \]
AC Testing Recorded in Real Time: $>10 \times 10^6$ Cycles

- Plotted above: 1,142,000 cycles
- Total cycles for this device so far: $>10$ Million Cycles
- Status: Still Alive, Preserved in Vacuum
- Also observed: “Resting” helps
Box (A)

Box (B)

Control

After >10^6 Cycles

On/Off >10^6
Very Encouraging for Small NEMS ↔ Benchmarking

Recorded Switching Cycles vs. Motional Volume (µm³)

Goal
This Work
This Work

Need Keep Updating
Lifetime & Reliability Challenges

Recorded Cycle Numbers
Motional Volume ($\mu$m$^3$)

Goal
This Work

High-Performance MEMS

Lifetime & Reliability Challenges

State-of-the-Art NEMS

Lifetime & Reliability Challenges

Recorded Cycle Numbers
Motional Volume ($\mu$m$^3$)
SiC NEMS Logic Switches

Results at High Temperature (500°C)

He, Yang, Feng, et al., IEEE MEMS 2013; IEEE IEDM 2013
Data from High-Temperature (500°C) Testing

- **FIB Salvaged Device**

- **Dual-Gate Device**

![Graphs and images illustrating data from high-temperature testing](attachment:image.png)
High-$T$ (500°C) Data from Last Night, Testing Still On

[Old] Spring 2012 Setup

[New] Cables are gone, all on a board which interfaces with (i) Triax from Analyzer; (ii) Coax from AC testing instruments
A Brief Outlook – Future Perspectives

Challenges & Opportunities
Next 1: Time-Resolved Probing of Switching Dynamics

- Lateral Si NEMS in Simulation:
  - $L=2 \mu m$, $w=100\text{nm}$, $t=100\text{nm}$
  - Coupling Gap=50nm
  - Switching Gap=20nm
  - Resonance $f_0=26.5\text{MHz}$
  - Step excitation: 8V

- Trade-off between the gap size and switching time
- Interesting dynamics: at contact, some beam modes are excited
- Future study may incorporate elasticity and surface effects
- Need to engineer suppression of “contact bounce”
Next 2: Complementing/Integrating with SiC JFET Circuits

### SiC

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>6H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap</td>
<td>1.1 eV</td>
<td>3.05 eV</td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>1.5 W cm(^{-1})K(^{-1})</td>
<td>4.9 W cm(^{-1})K(^{-1})</td>
</tr>
<tr>
<td>Elastic Modulus</td>
<td>~150 GPa</td>
<td>~400 GPa</td>
</tr>
</tbody>
</table>

### SiC JFET

- p-n junction gate
- No gate insulator that can degrade
- “Normally on” (a lot of leakage!)
- Must deplete the entire channel thickness to “turn off” the device

### Scaling is Greatly Desired but Hard

<table>
<thead>
<tr>
<th>Spec</th>
<th>(W/L = 200\mu m/10\mu m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_t)</td>
<td>-11.8 V</td>
</tr>
<tr>
<td>(I_{DSS})</td>
<td>1.32 mA</td>
</tr>
<tr>
<td>(I_{off})</td>
<td>0.09 (\mu A)</td>
</tr>
</tbody>
</table>
**Next 3: Ultra-Light-Mass Materials?**

Graphene NEMS with On-Chip Electronic Controls
Graphene NEMS Examples: 2-Terminal, Vertical

- Bilayer Graphene, $t \approx 0.68\text{nm}$; $g \approx 300\text{nm}$, $V_{\text{on}} \approx 4\text{V}$, $L \approx 3\mu\text{m}$, $w \approx 1\mu\text{m}$
TMDCs \( \rightarrow \) Very High Frequency (VHF) MoS\(_2\) Resonators

Smaller Resonator \( \rightarrow \) VHF

- \( d=1.5-2\mu m \)
- \( t=6.1\) (9 layers)-62.2nm
- Fully covered
- Incompletely covered
- Sensitivity=40-250fm/Hz\(^{1/2}\)

High Frequency MoS$_2$ Nanomechanical Resonators

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ABSTRACT Molybdenum disulfide (MoS$_2$), a layered semiconducting material in transition metal dichalcogenides (TMDCs), as thin as a monolayer (consisting of a hexagonal plane of Mo atoms covalently bonded and sandwiched between two planes of S atoms, in a trigonal prismatic structure), has demonstrated unique properties and strong promises for emerging two-dimensional (2D) nanodevices. Here we report on the demonstration of movable and vibrating MoS$_2$ nanodevices, where MoS$_2$ diaphragms as thin as 6 nm (a stack of 9 monolayers) exhibit fundamental-mode nanomechanical resonances up to $f_0 \sim 60$ MHz in the very high frequency (VHF) band, and frequency-quality ($Q$) factor products up to $f_0 \times Q \sim 2 \times 10^{10}$ Hz, all at room temperature. The experimental results from many devices with a wide range of thicknesses and lateral sizes, in combination with theoretical analysis, quantitatively elucidate the elastic transition regimes in these ultrathin MoS$_2$ nanomechanical resonators. We further delineate a roadmap for scaling MoS$_2$ 2D resonators and transducers toward microwave frequencies. This study also opens up possibilities for new classes of vibratory devices to exploit strain- and dynamics-engineered ultrathin semiconducting 2D crystals.

KEYWORDS: two-dimensional (2D) crystals · molybdenum disulfide (MoS$_2$) · nanoelectromechanical systems (NEMS) · resonators · thermomechanical noise · frequency scaling · displacement sensitivity
Summary & Outlook – Promising SiC NEMS Logic

- **SiC NEMS**: Demonstrated New Generations of
  - Robust, Long-Lifetime SiC NEMS Logic Switches
  - High-Temperature 500°C Operations of NEMS Logic Switches
  - Low-Voltage SiC NEMS Switches → FPGA
  - SiC NEMS Inverters and Sub-Circuits

- Ongoing & Future Extensive Efforts on Devices Contacts Studies
  - Control Testing Conditions
  - Speeding Up Toward Intrinsic Speeds of SiC NEMS

- Many Interesting & Promising Opportunities
  - Optimized Designs, from Lessons Learned from Recent Devices
  - New Fabrication Techniques → High-Yield Wafers
  - Toward Intrinsic Lifetimes and Very Large Scale Integration
...I’ve been privileged... Feng Group @ Case
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