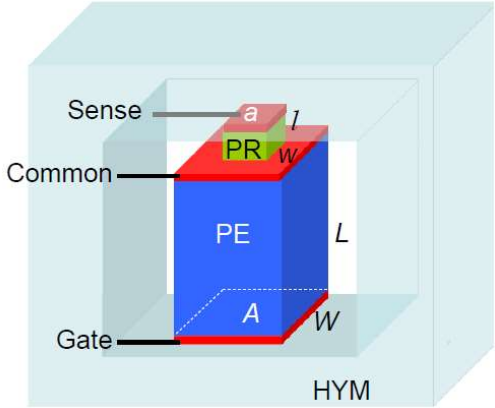
The Piezoelectronic Transistor

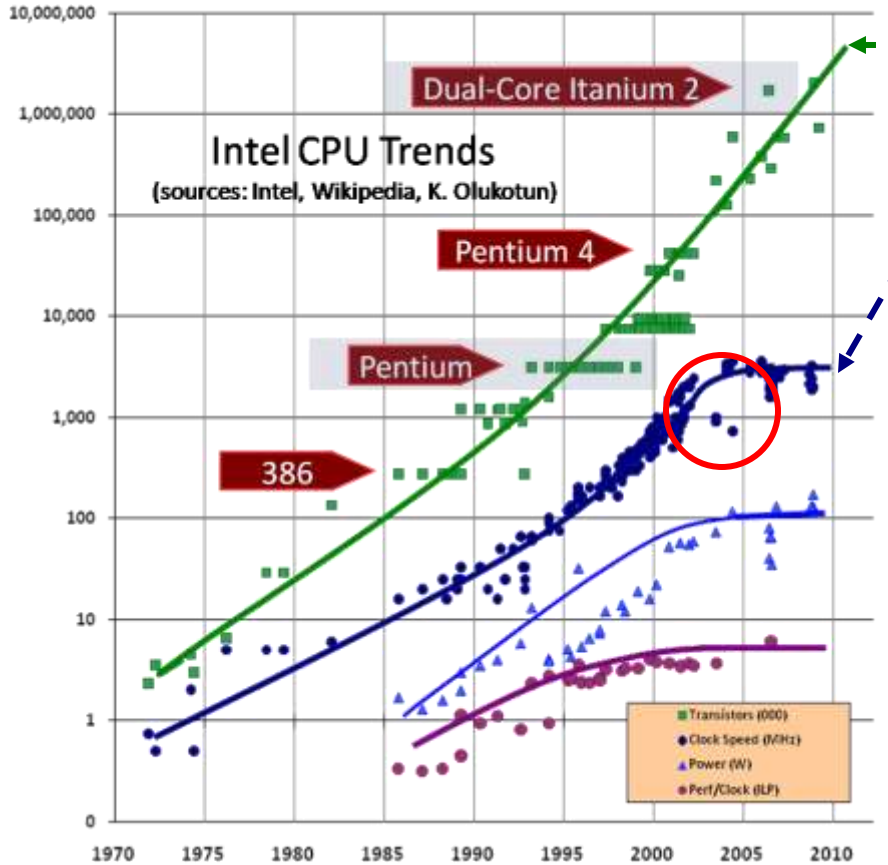


The PiezoElectronic Transistor (PET)

PI: Dennis Newns
Theory: *Glenn Martyna, Bruce Elmegreen, Xiao-Hu Liu, Marcelo Kuroda*
Experiment: *Paul Solomon, Brian Bryce, Li-Wen Hung, Matt Copel, Alejandro Schrott, Wilfried Haensch, Chang-Beom Eom, Stephen Rossnagel, Thomas Shaw, Hiroyuki Miyazoe, Ryan Keech, Smitha Shetty, Susan Trolier-McKinstry*

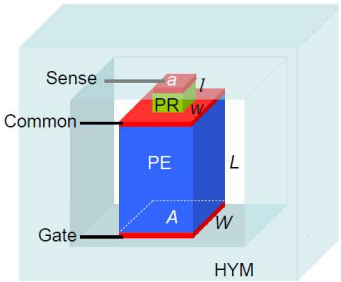
Motivation – Overcome CMOS Speed Block

Moore's Law



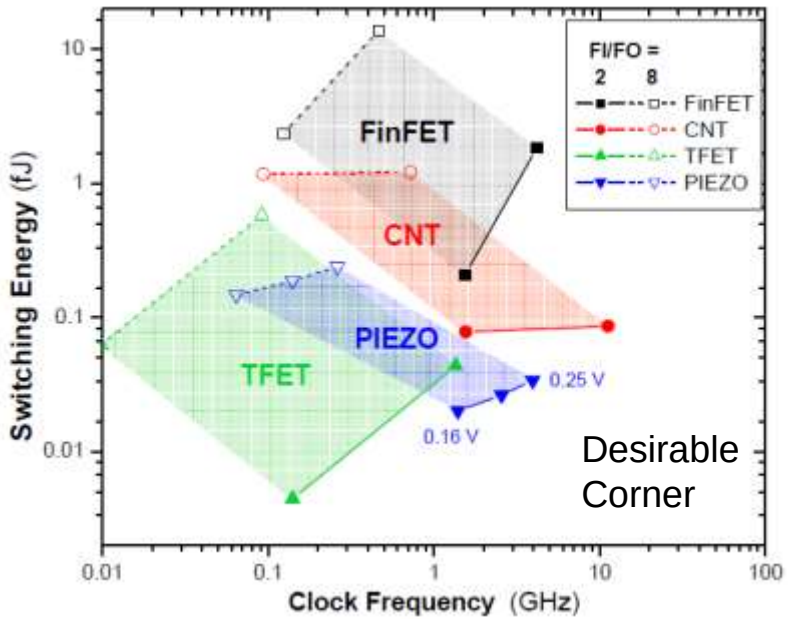
Moore's Law: transistor density is *still increasing*

- But CMOS clock speed has **not increased** since 2003– limiting processor compute power
- Line voltage V_{DD} has **stopped decreasing** so power rises unacceptably if speed increases.
- Invent a new type of fast switch with novel physics operable at **low voltage/power**
- Our PiezoElectronic Transistor (PET) is shown by simulation and theory (based on bulk material properties) to achieve this goal.

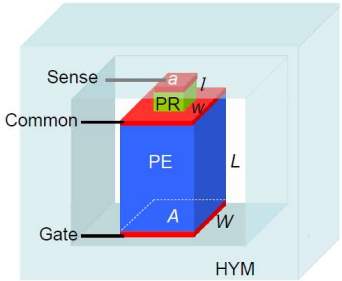


Reduce *server farm, supercomputer, hand-held device* power consumption.

Comparative PET Performance



11nm Technology study:
The PET has impressive advantages!



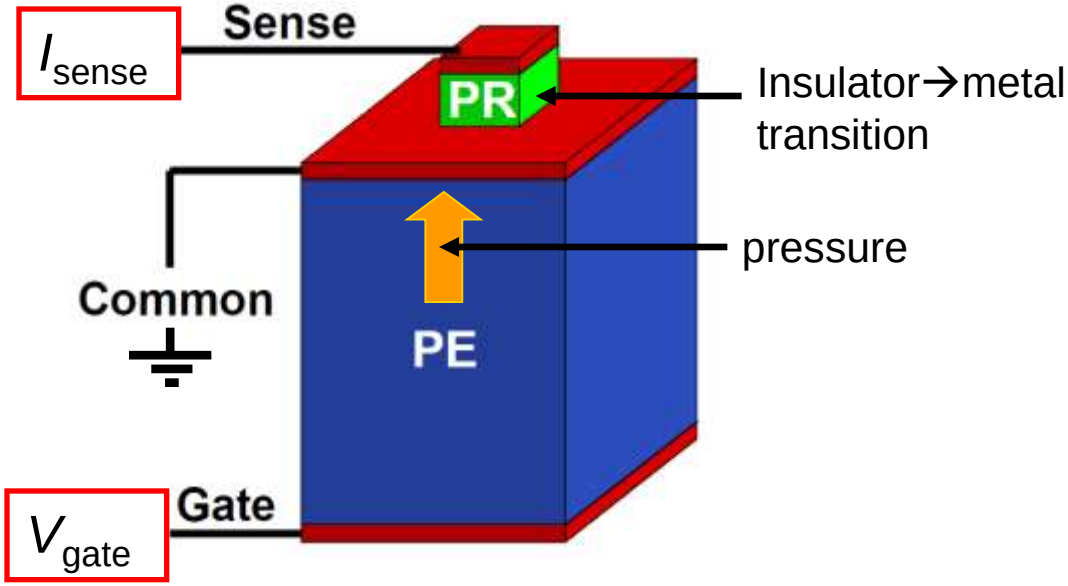
PET low power, high speed, performance compares favorably with other Switching devices. Fanout supported.

Power up to factor of 50 saved over the FinFET.

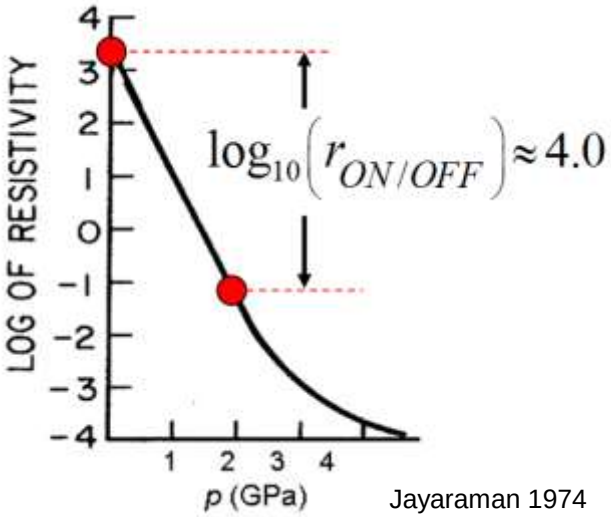
CNT and TFETs not yet realized.

Piezotronics - Electrical Viewpoint

A ***gate*** voltage on a ***piezoelectric*** (PE) applies ***pressure*** to a ***piezoresistive*** (PR) material which induces a **insulator→metal transition**, turning on the current through ***sense***.



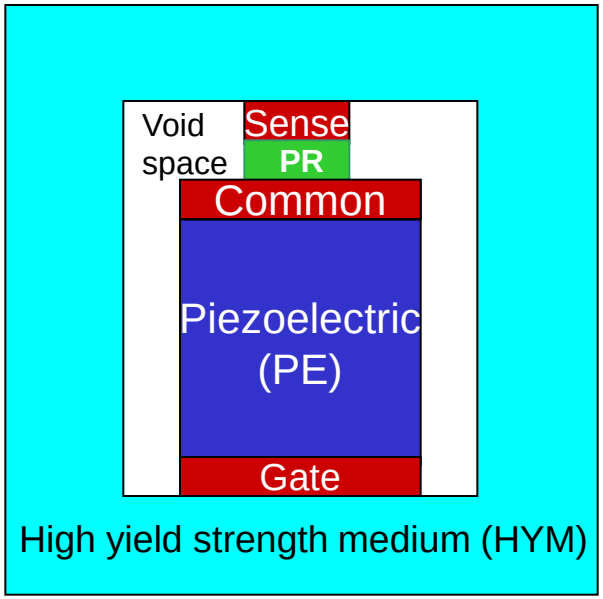
Piezoelectronic Transistor (PET)

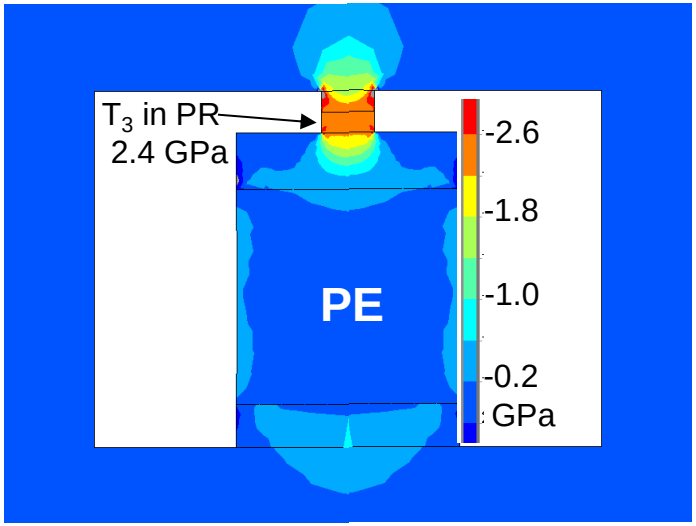


Jayaraman 1974

Straightforward structure for fabrication at industry scales with current litho approaches, but *materials are unconventional* (though well-characterized in bulk).

Piezotronics – Mechanical Viewpoint





The Gate/PE/Common/PR/Sense sandwich is embedded in a **high yield strength medium** (HYM; e.g., SiN), to hold the Sense-Drive physical distance constant.

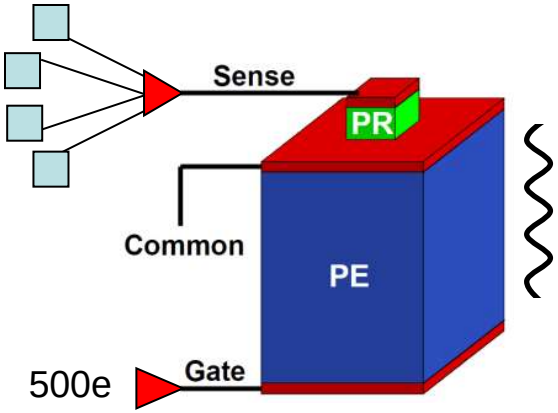
The area ratio $Area_{PR} << Area_{PE}$ (a/A) steps up the pressure in the PR – the **hammer and nail principle.**

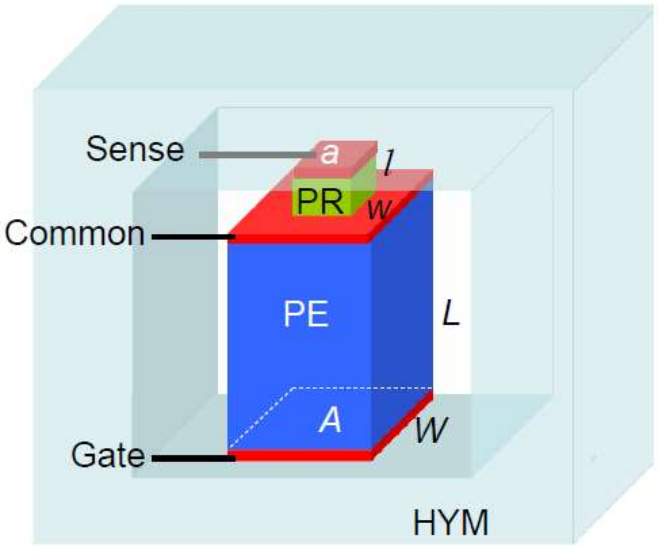
A void space allows unconstrained motion of the components.

Piezotronics has a *unique* set of advantages:

- **Complete technology**
- **Low power**
- **Speed – ps time scale**
- **Low Noise**
- **Scalable** – follows Dennard Scaling Law
- **High Fan out**

IBM's Bob Dennard

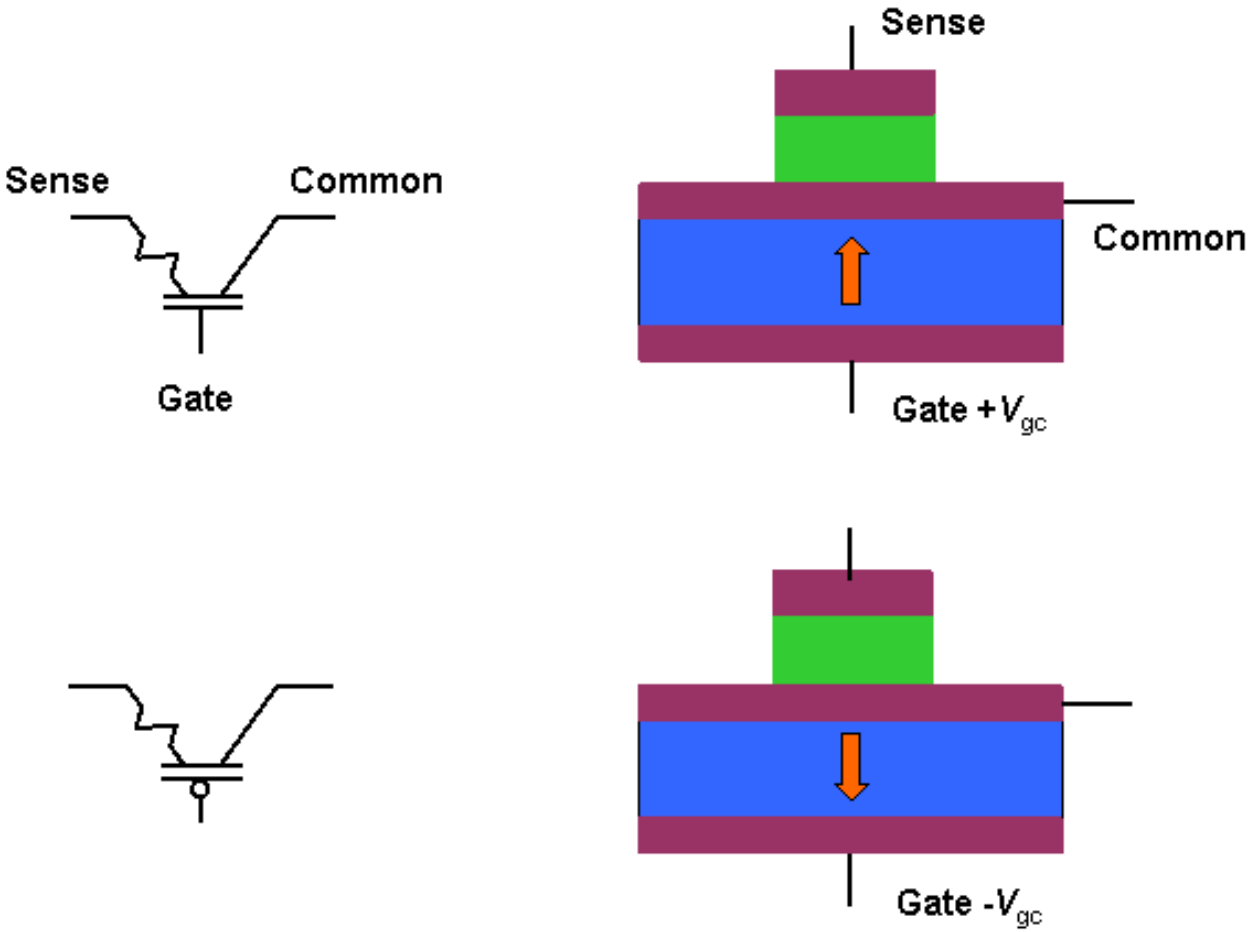




PET Logic and Theoretical Perfomance

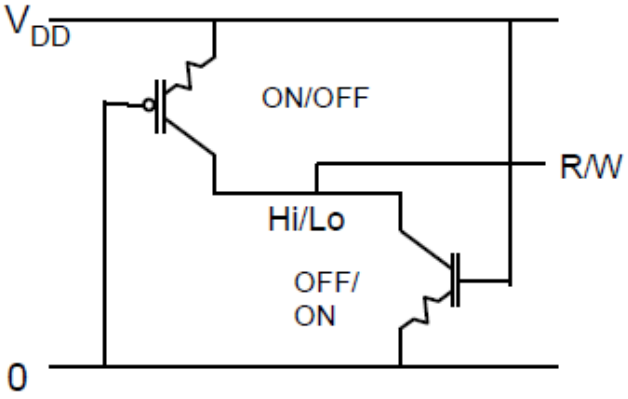
COMPLEMENTARY PETS

For computer circuits need *complementary* PET devices.

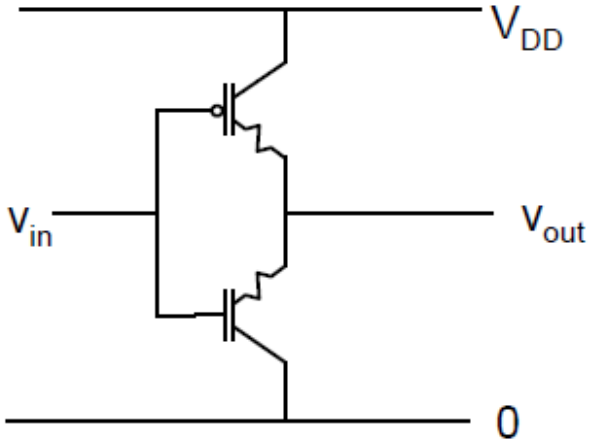


One approach is to pole the PE oppositely, generating complementary devices.

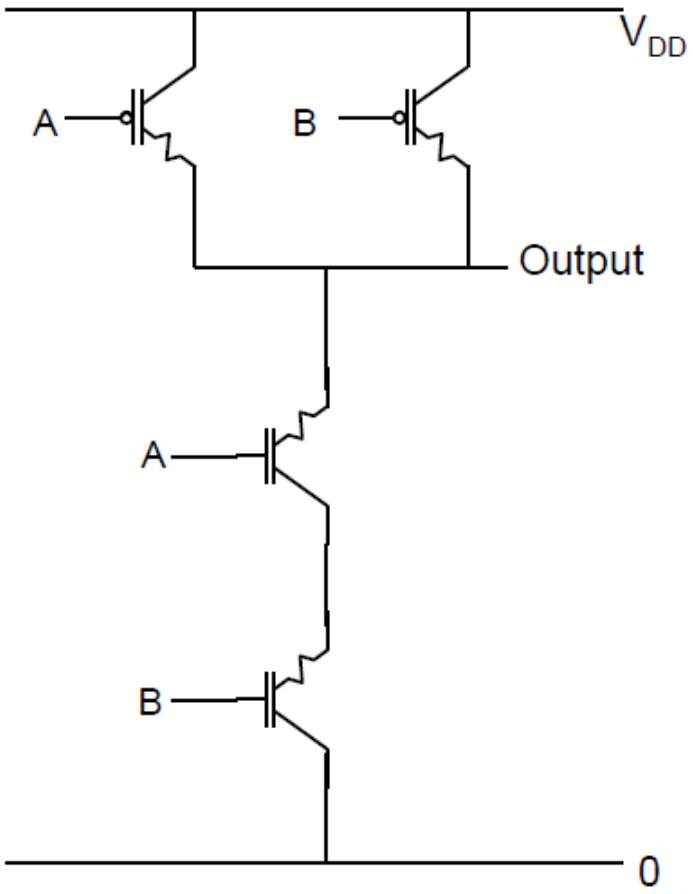
Piezotronics can build any logic circuit



Bistable PET Flip-Flop → 4 transistor SRAM

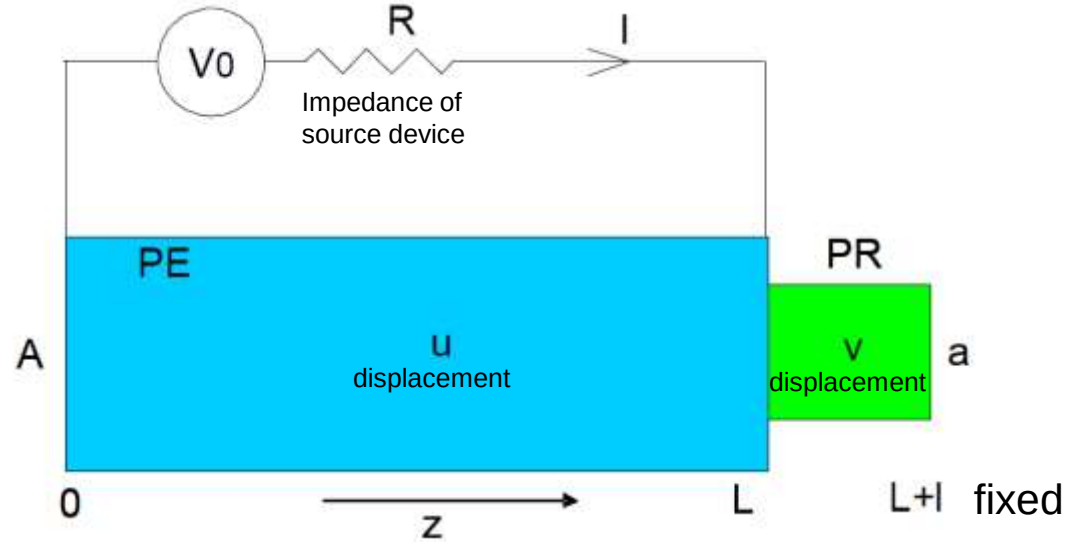


PET inverter



PET NAND gate

PET 1D Modeling to investigate performance



Piezo terms

Stress $$T(z,t) = c^E \frac{du(z,t)}{dz} - \boxed{e^t E(z,t)}$$

Surface charge density $$\sigma(t) = \boxed{e\frac{du(z,t)}{dz}} + \epsilon^S E(z,t).$$

$$\frac{\partial T(z,t)}{\partial z} = \rho \frac{\partial^2 u(z,t)}{\partial t^2}$$

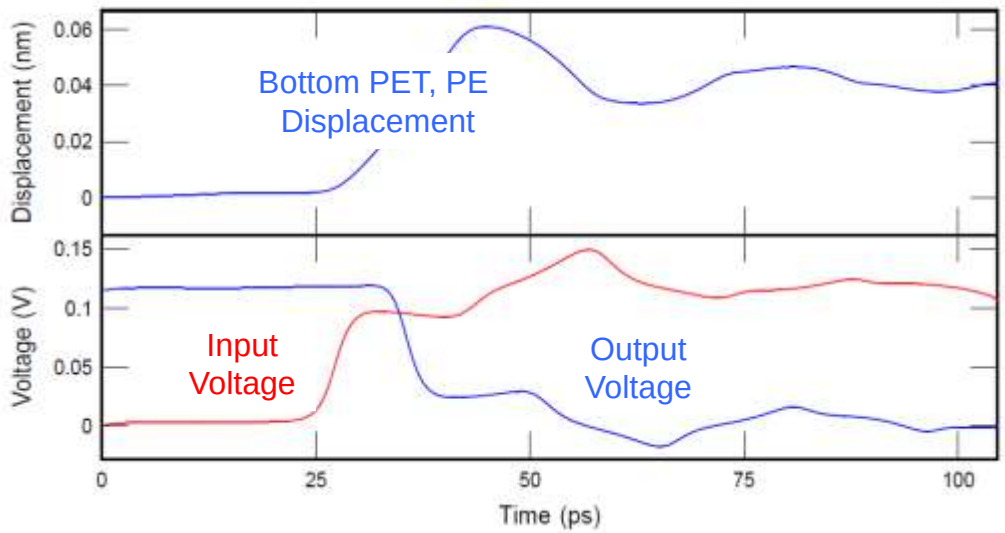
$$T'(z,t) = c^{E'} \frac{dv(z,t)}{dz},$$

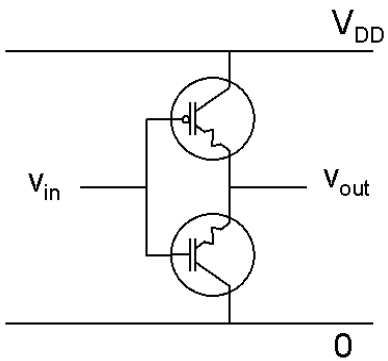
$$\frac{\partial T'(z,t)}{\partial z} = \rho' \frac{\partial^2 v(z,t)}{\partial t^2}$$

Coupling constant *g* $$g = (c^E d_{33}^2)/\epsilon^S$$

c^E = Young's modulus, d_{33} = Piezo-coefficient nm/volt,
$e = d_{33}c^E$, ε^S=dielectric constant at constant strain, ρ=density

Switching Single PET Inverter





Energy:

- at scale a few aJ

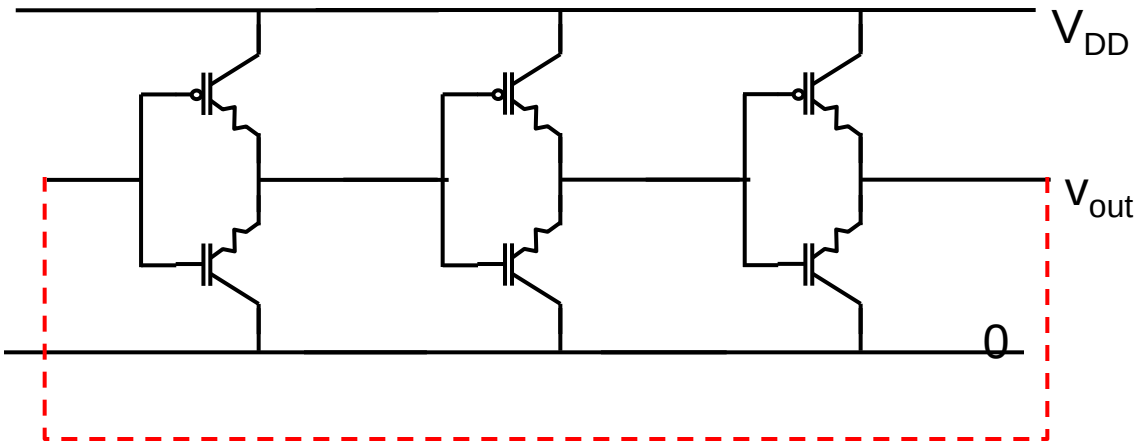
At inverter switch-ON:

- PE displacement transition is underdamped (R_{PR} provides only damping in model)
- The PE *charges* from source device in τ_{RC}
- The PE *expands* in $\tau_{sonic} = L_{PE} / v_{sound}$

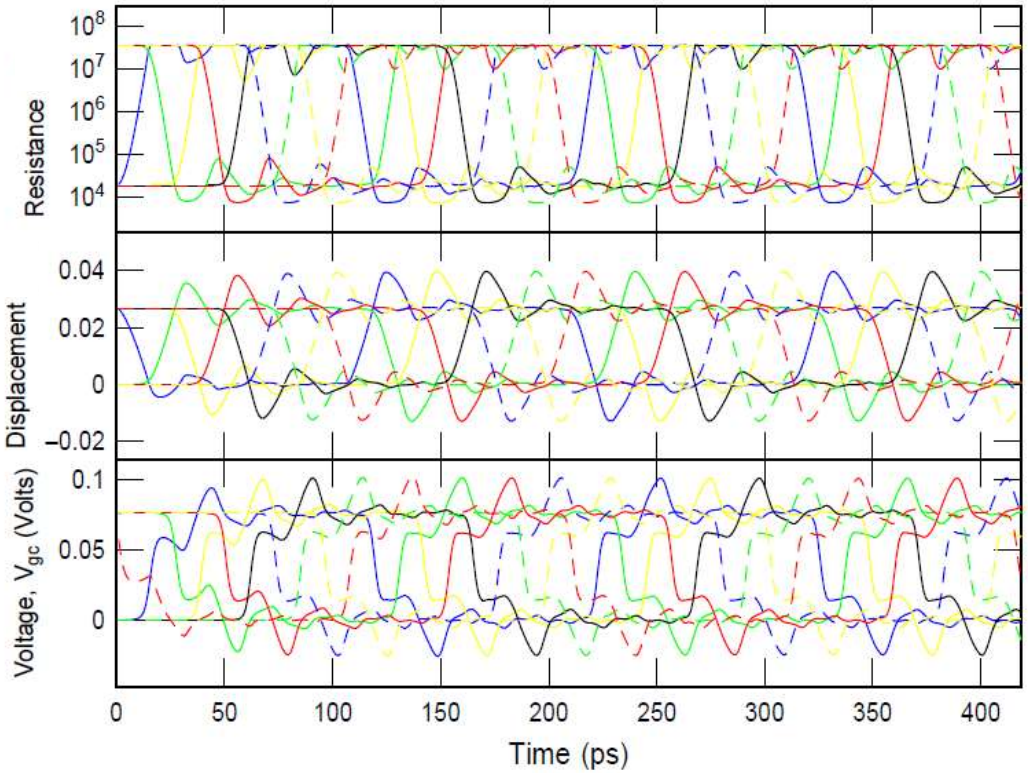
D.M. Newns, B.G. Elmegreen, X-H Liu and G.J. Martyna, *JAP.* 2012

Ring Oscillator

Chain of inverters
plus
Feedback loop



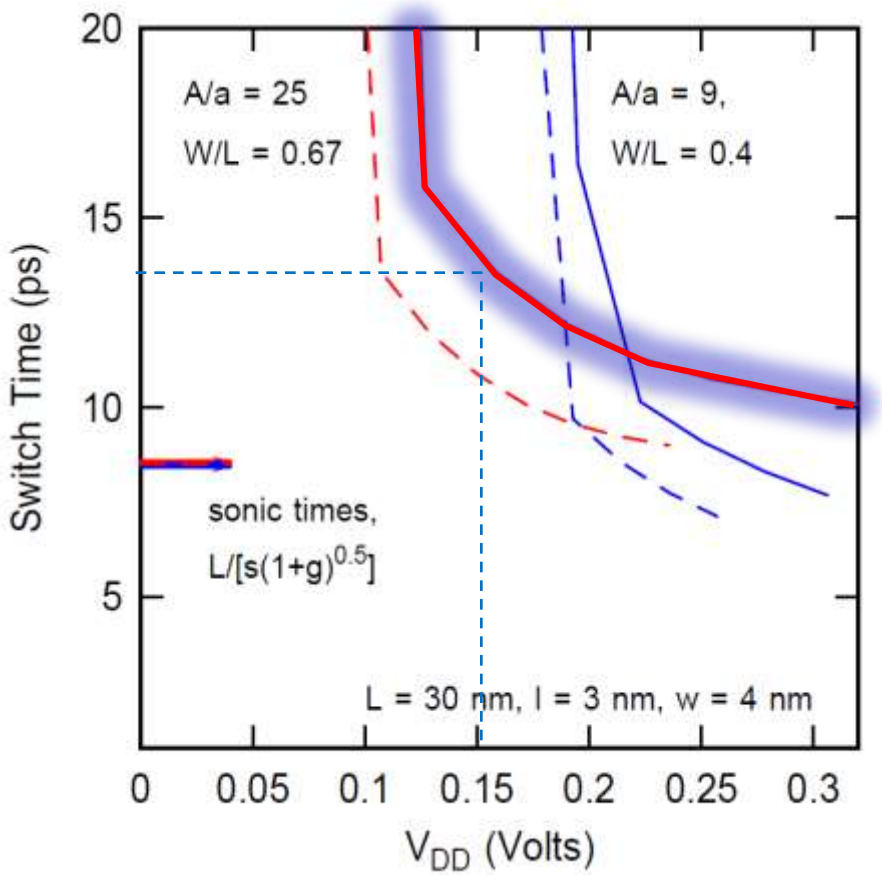
Output V of Each Stage
(9 stages)

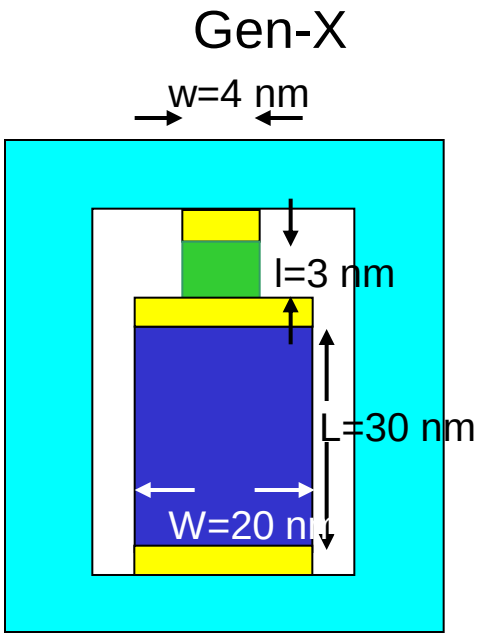


9 stage RO, V_{dd}=0.076 V, R_{ON}/R_{OFF}=5000, A/a=25, W/L=0.75, 45 GHz

L = 26.666 nm, W = 20 nm, w = 4 nm, l = 2 nm

The Piezoelectronic Transistor at Ultimate Scale





PET corresponding to red curve

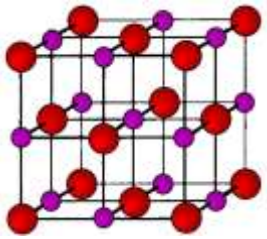
Bruce Elmegreen, based on Kuroda-Martyna multiscale model and measured bulk properties

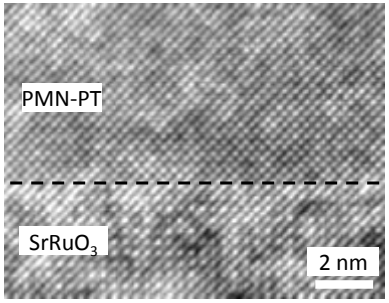
Materials

PR

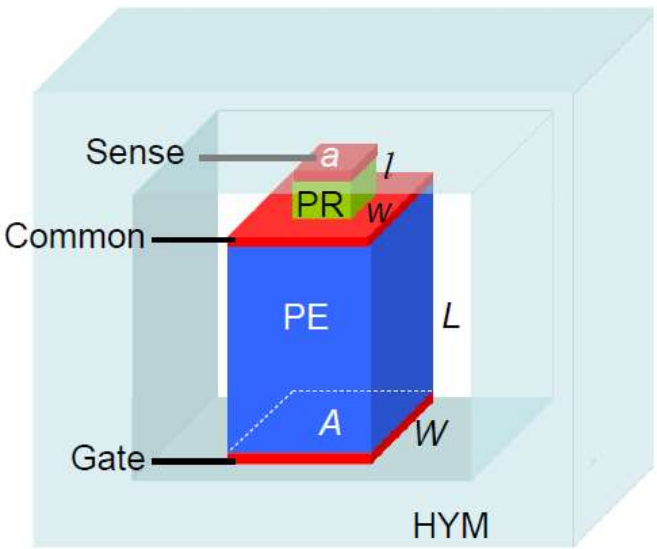
PE

SmSe



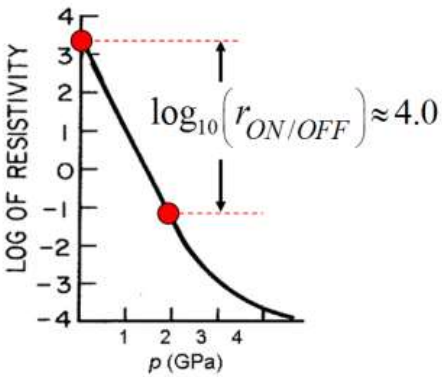


Materials are Critical to Achieving PET Performance



Piezoresistor

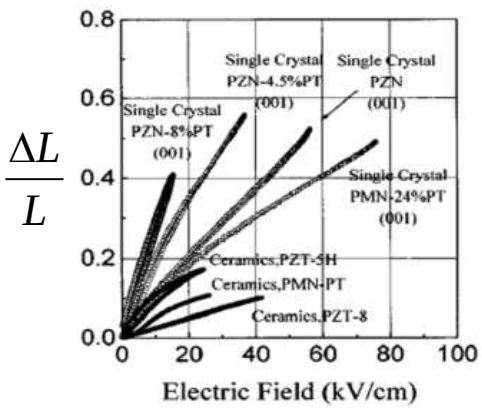
- To get adequate ON/OFF ratio need high PR pressure
- aided by high slope



$$p_{PR} \approx \frac{d_{33}^{PE} V_G}{\frac{l}{Y_{PR}} + \left(\frac{a}{A}\right)\frac{L}{Y_{PE}}}$$

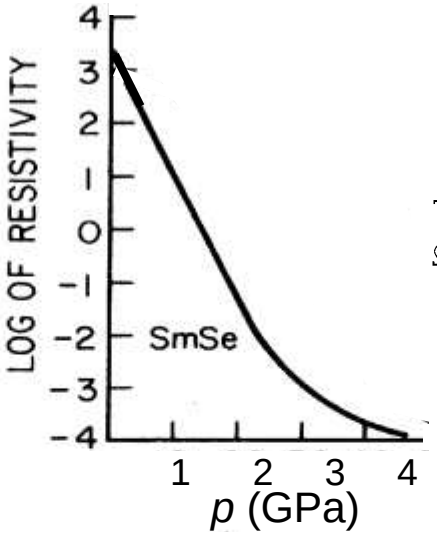
Piezoelectric

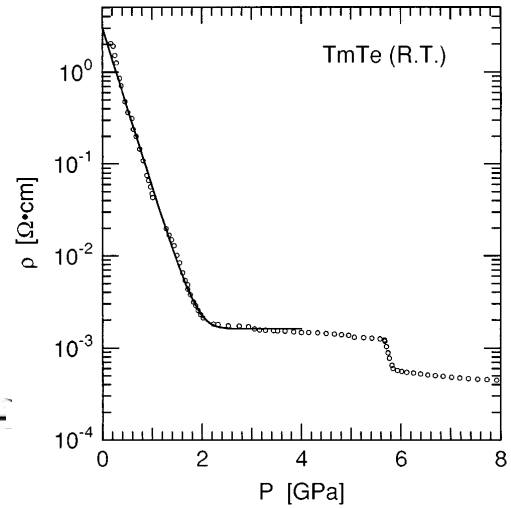
- To achieve at low voltage
- need high PE sensitivity d_{33}^{PE}
- materials operable at small scale *L, l*



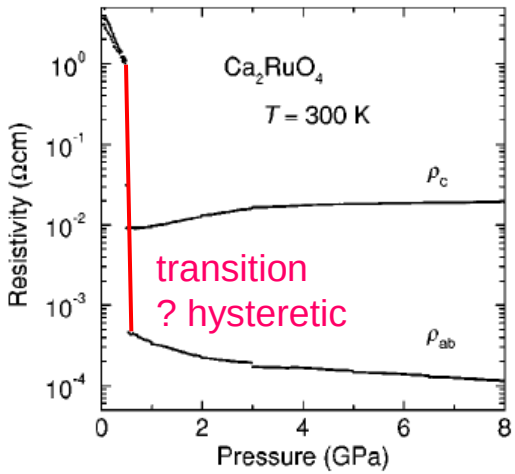
PR selection – Two Classes of Materials

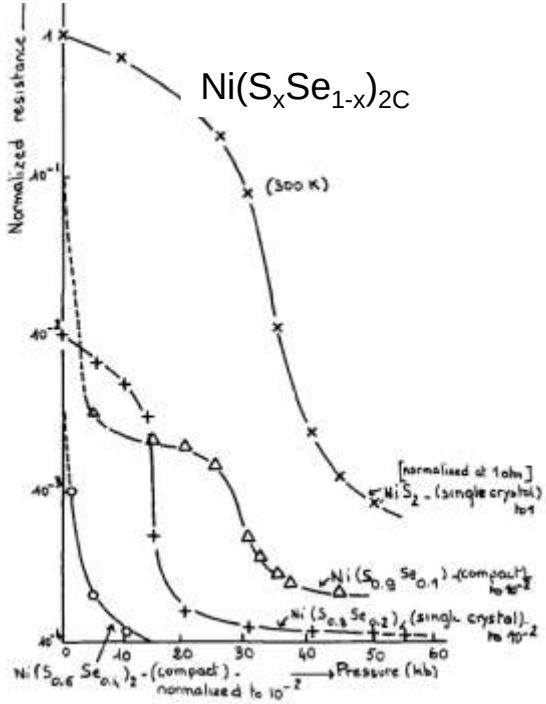
Rare Earth
Intermediate
Valence

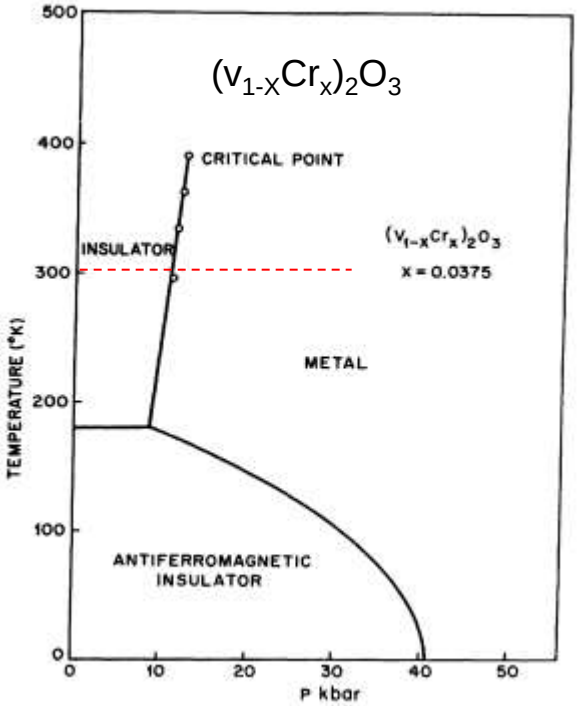




Mott Transition

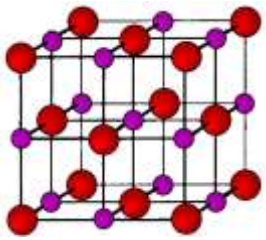






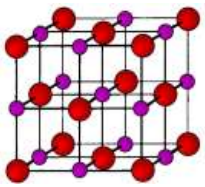
SmSe – Pressure controlled Dopant Level

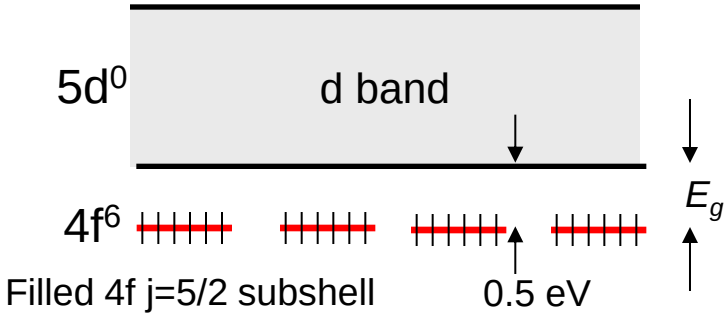
SmSe

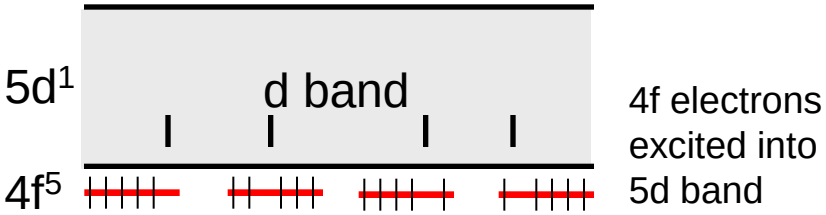


Rocksalt structure

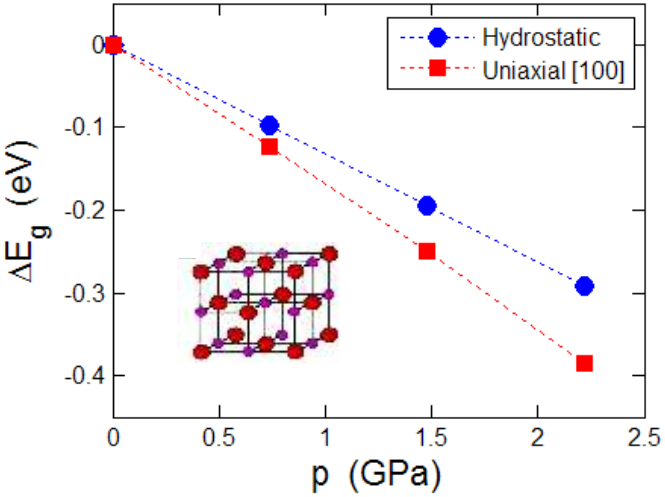
SmSe, Hydrostatic Compression







Pressure promotes 4f electron energy

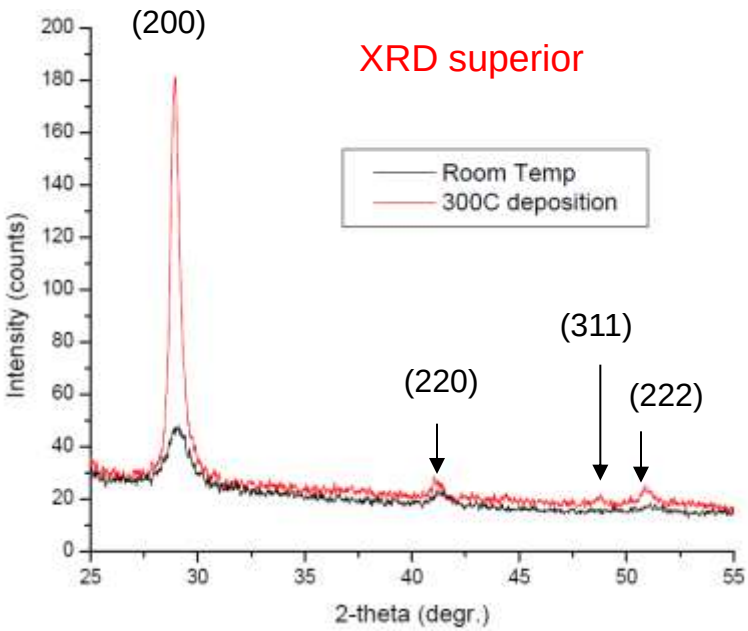


- *Ab Initio* Modeling shows reduction in 4f-5d gap *Eg* under stress
- Gap narrowing **greater for anisotropic stress**
- Can fit gap under anisotropic stress to

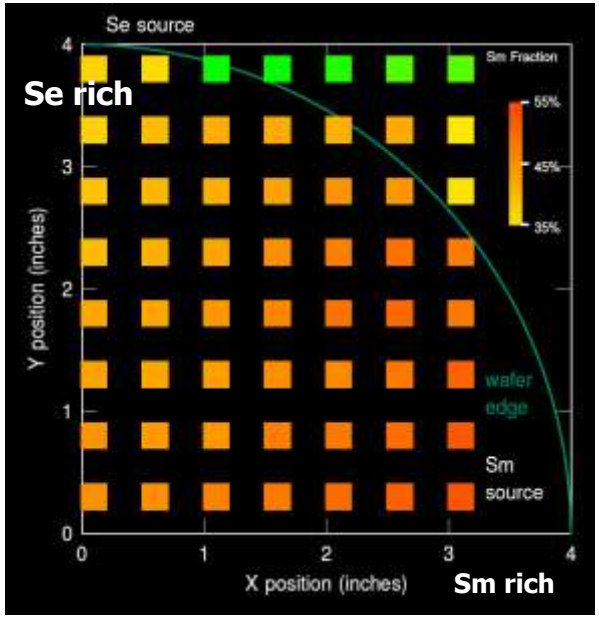
$$E_g = \alpha T_{\square} + \beta T_{\perp}; \text{ where } T = \text{stress}$$

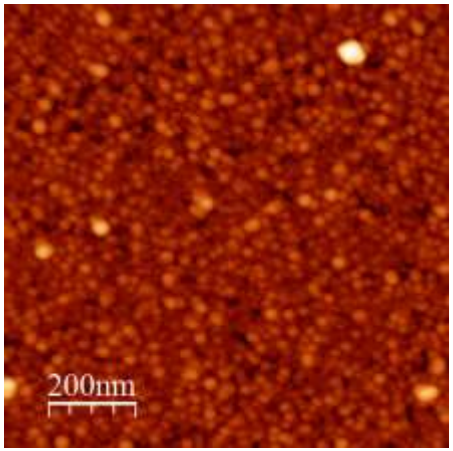
so gap known in *realistic strain* environment
- enabling PET performance prediction

Hot Deposition and Compositional Grading of Sputtered 50 nm SmSe film



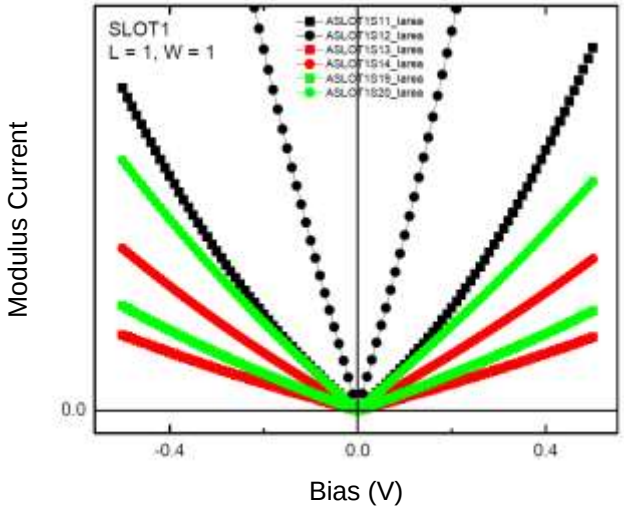
Compositional grading for materials development





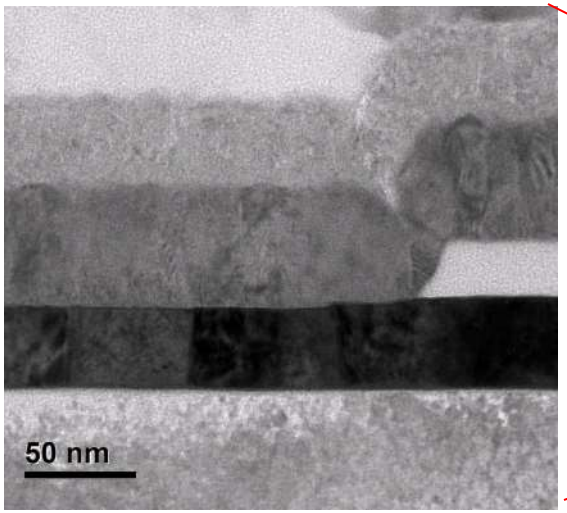
IV characteristics are close to linear!

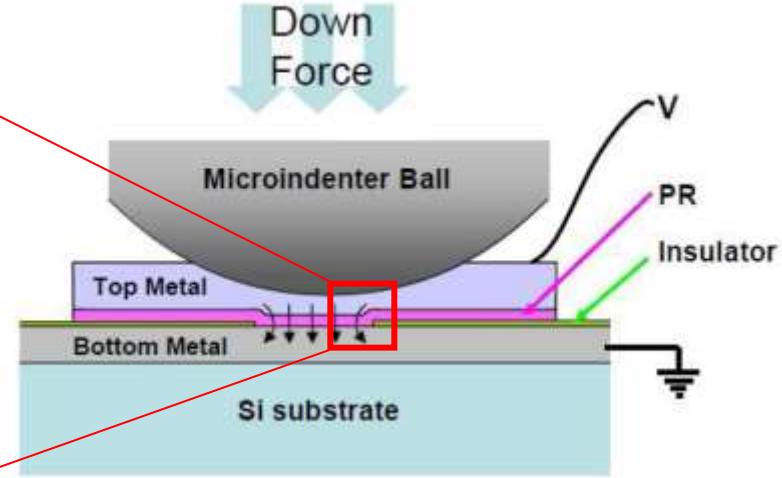
AFM scan shows fine-grained polycrystal



Sputtered 50 nm SmTe Films

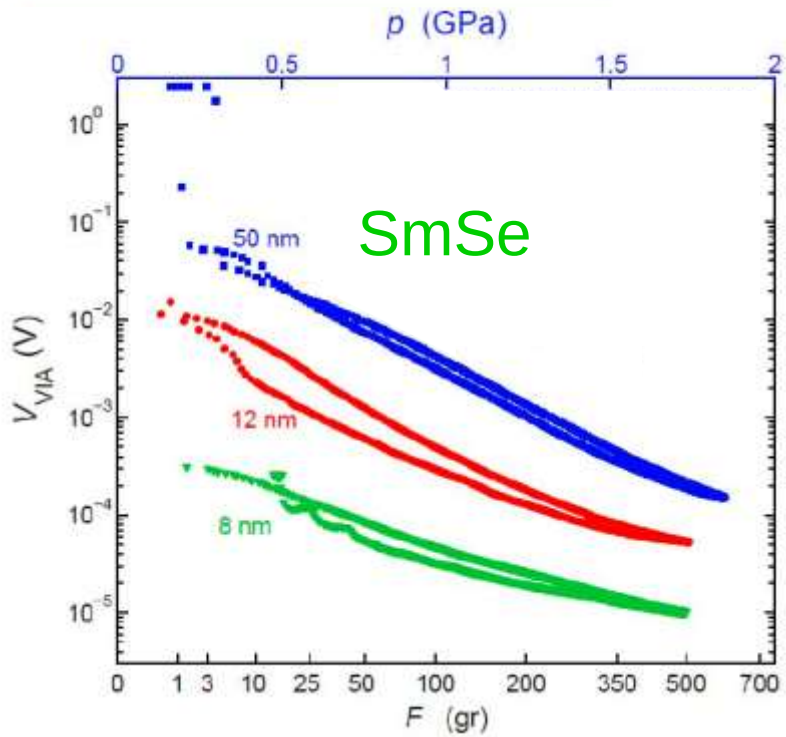
Novel Microindenter Experiment



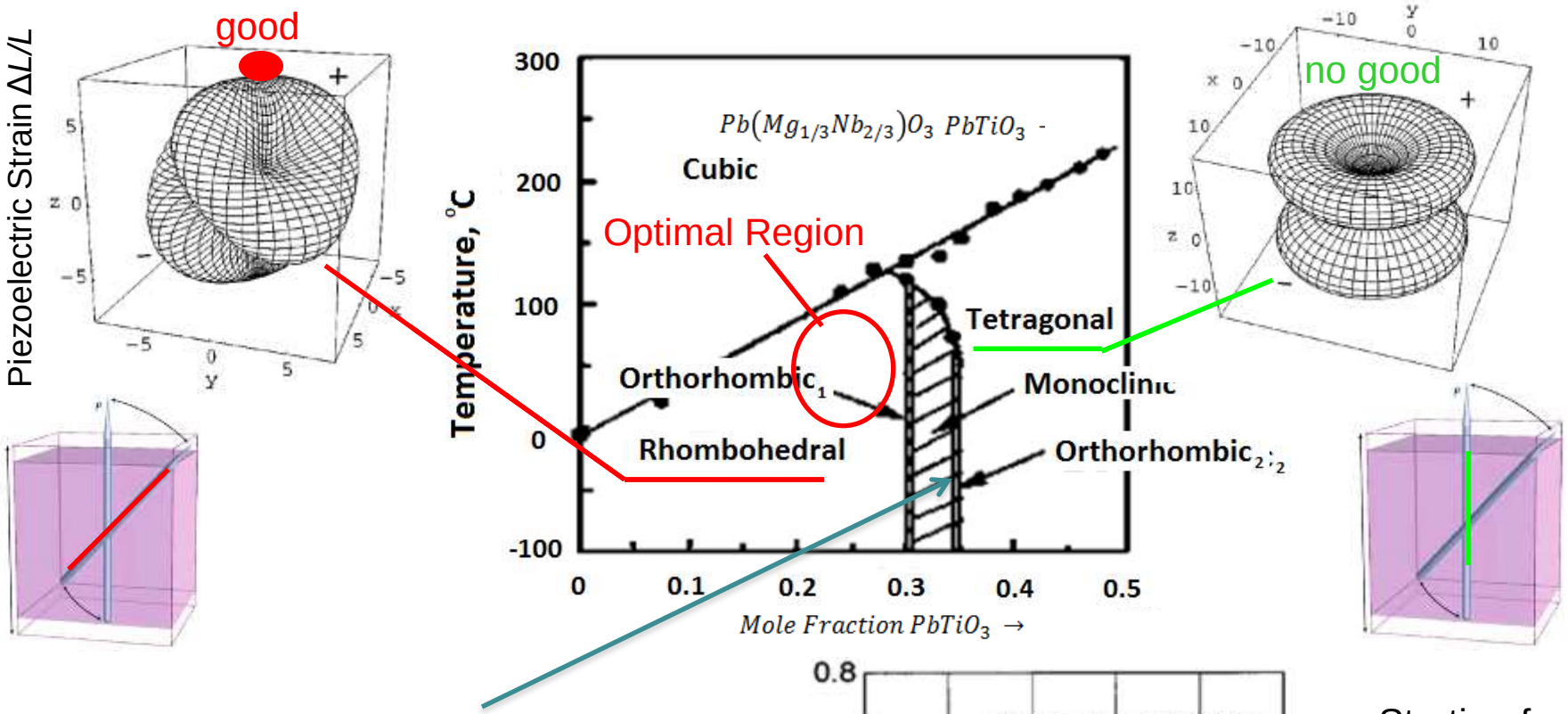


- High pressure (GPa range)
- Current flow transverse to film
- Via-confined current flow allows quantitative data analysis
- Pressure vs load calculated by Hertzian mechanics

- 2.5 orders of magnitude resistance change with pressure achieved.

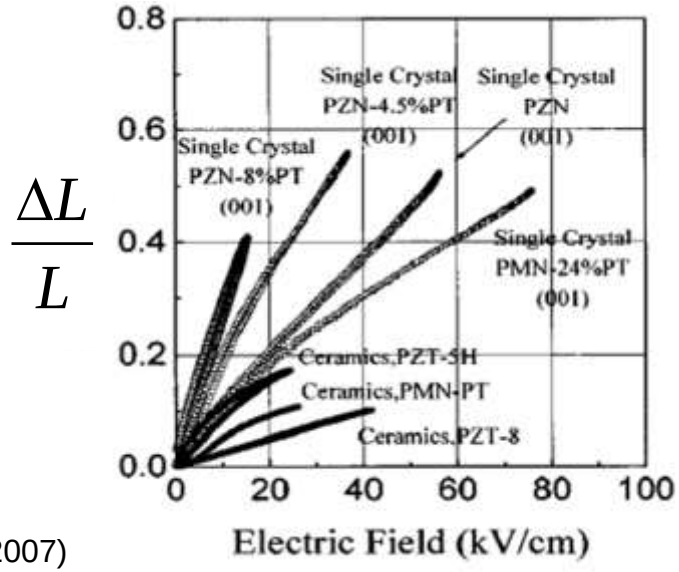


Relaxor PE's (e.g. PMN-PT) work by polarization rotation



- Near Morphotropic Phase Boundary, polarization can easily rotate from <111> in the rhombohedral phase towards [001] when the electric field is applied parallel to [001]

- This leads to a large piezo-effect along [001]

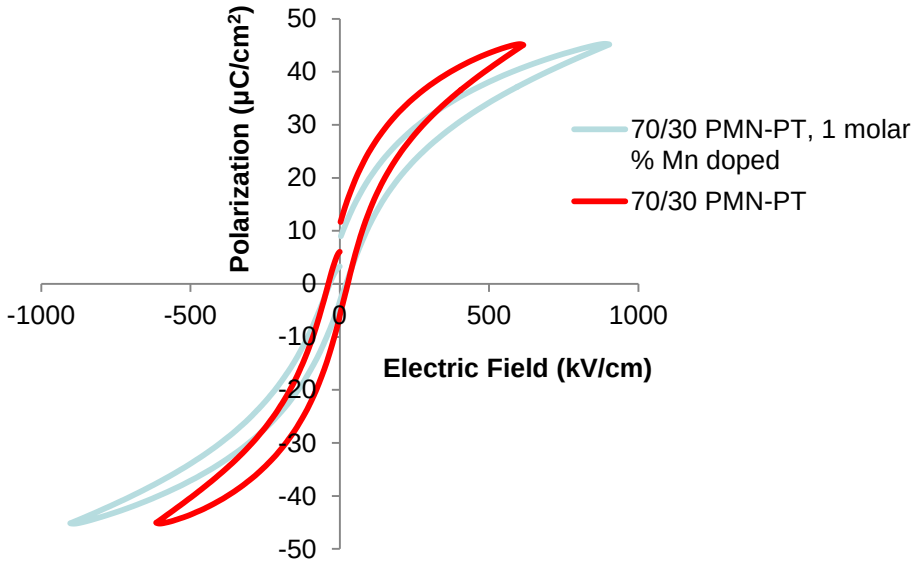


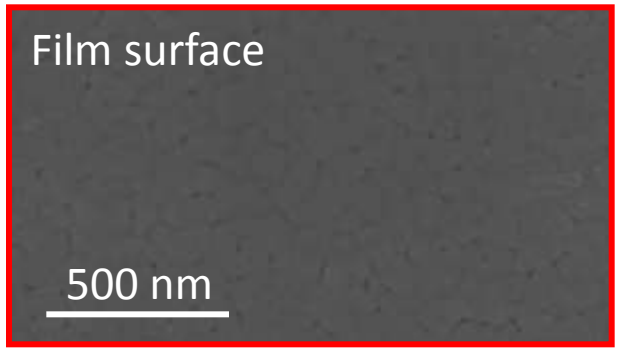
- Starting from tetragonal, there is no polarization rotation along [001], since the polarization is *already* directed along [001].

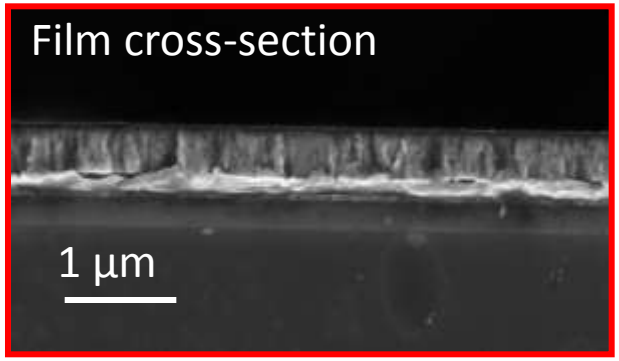
M.Iwata, Ferroelectrics, (2002), M. Davis et al., JAP (2007)

Chemical Solution Deposition of Large Area PMN-PT Films at PSU

Polarization vs. Applied Field Hysteresis Loop for PMN-PT films (~350 nm thick)



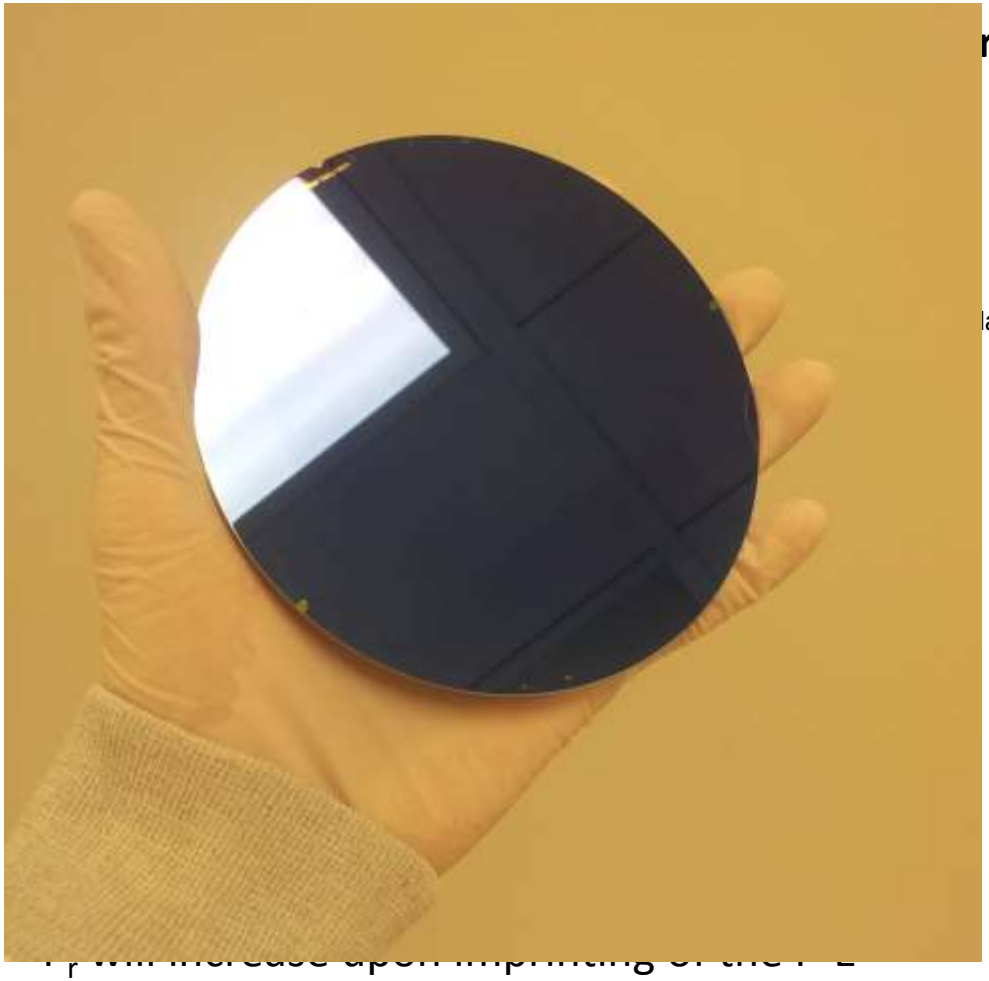




- P_r = 11 μC/cm², E_c = 33 kV/cm, ε_r = 2000
- Dense, columnar microstructure
- P_r will increase upon imprinting of the P-E loop

- High quality films now on 8” substrates
- Adequate piezoelectric coefficients / high fields achievable for test devices
- S. Trolier-McKinstry et al, Penn State

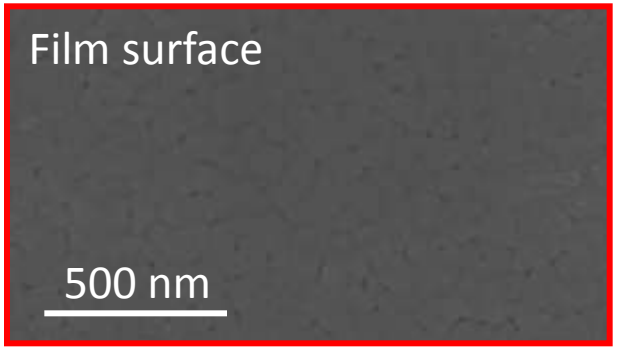
Chemical Solution Deposition of Large Area PMN-PT Films at PSU

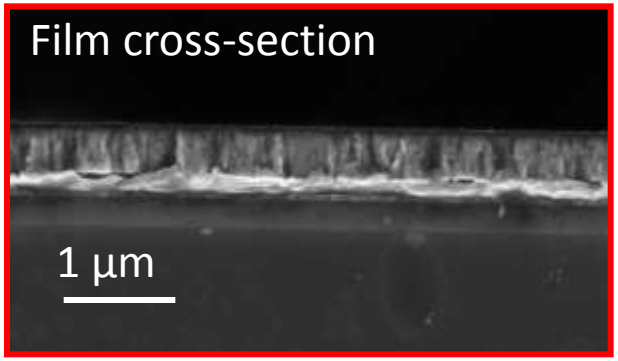


r

lar

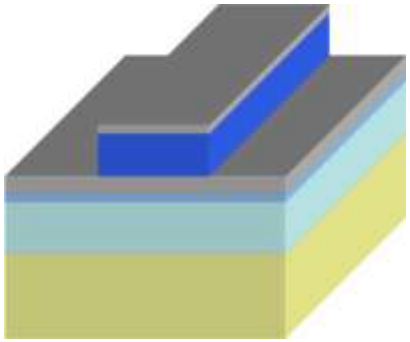
loop





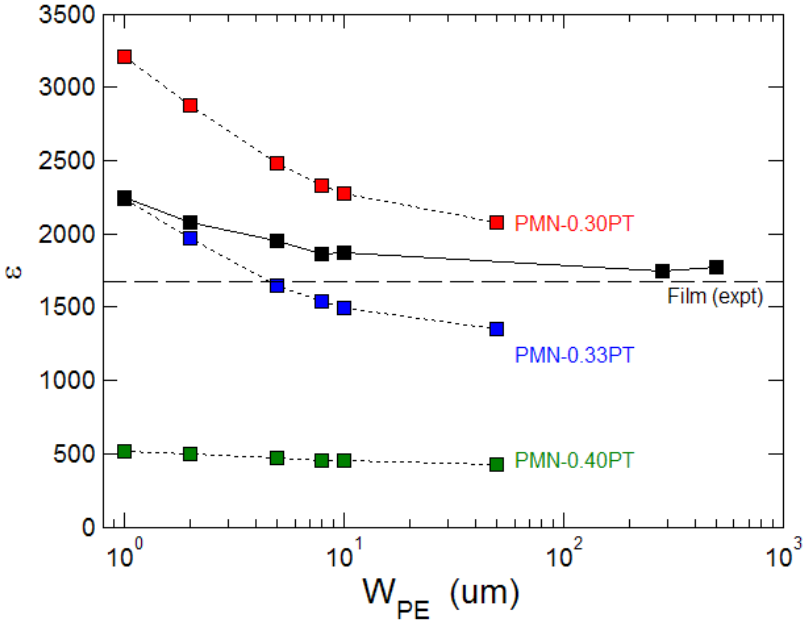
- High quality films now on 8” substrates
- Adequate piezoelectric coefficients / high fields achievable for test devices
- S. Trolier-McKinstry et al, Penn State

Dielectric Constant



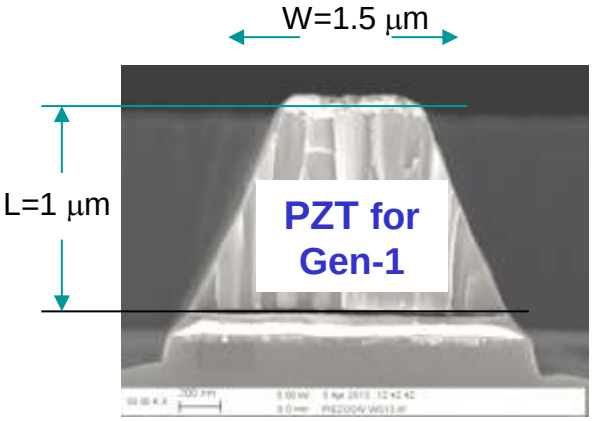
Conclusions:

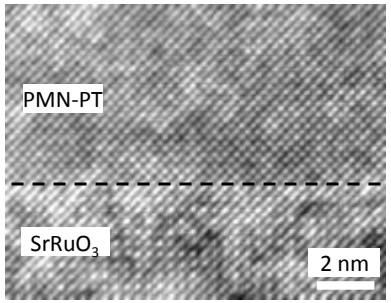
- Estimated effective dielectric constant in experiments (PSU) fall between expected values for x=0.30 and x =0.33 single crystals
- Increase of effective dielectric constant with reduction of antenna width not as rapid as ideally model, suggesting small degradation of piezoelectric response after etching

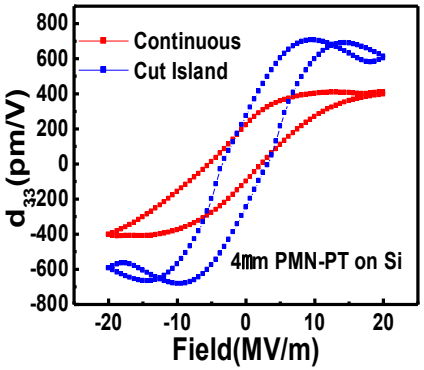


Improving PE Materials

Textured PZT → Epitaxial PMN-PT → Single Xtal PMN-PT





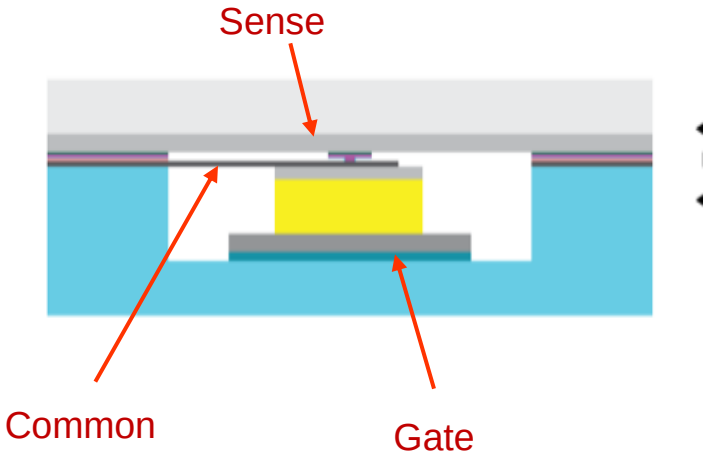


d_{33} (pm/V)	170

d_{33} (pm/V)	600 2x more expected

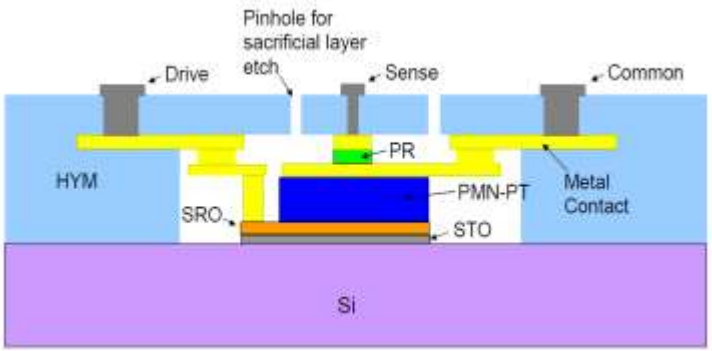
d_{33} (pm/V)	2820

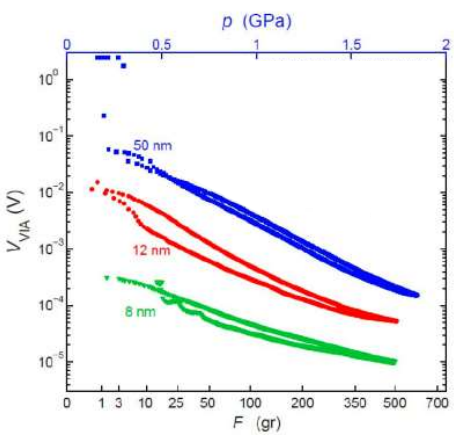
C.B. Eom et al.

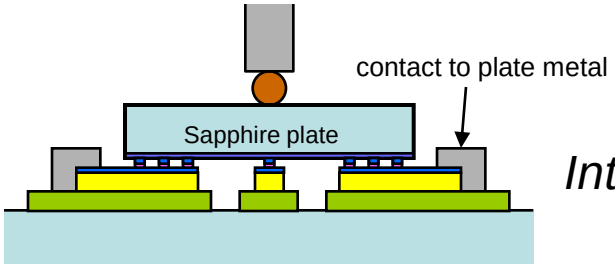


Devices

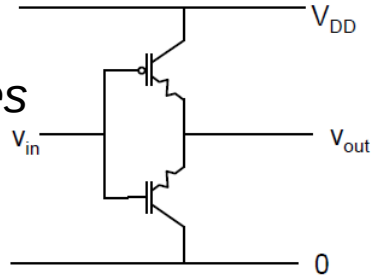
Piezotronic Development Plan







Integrated Devices and Circuits



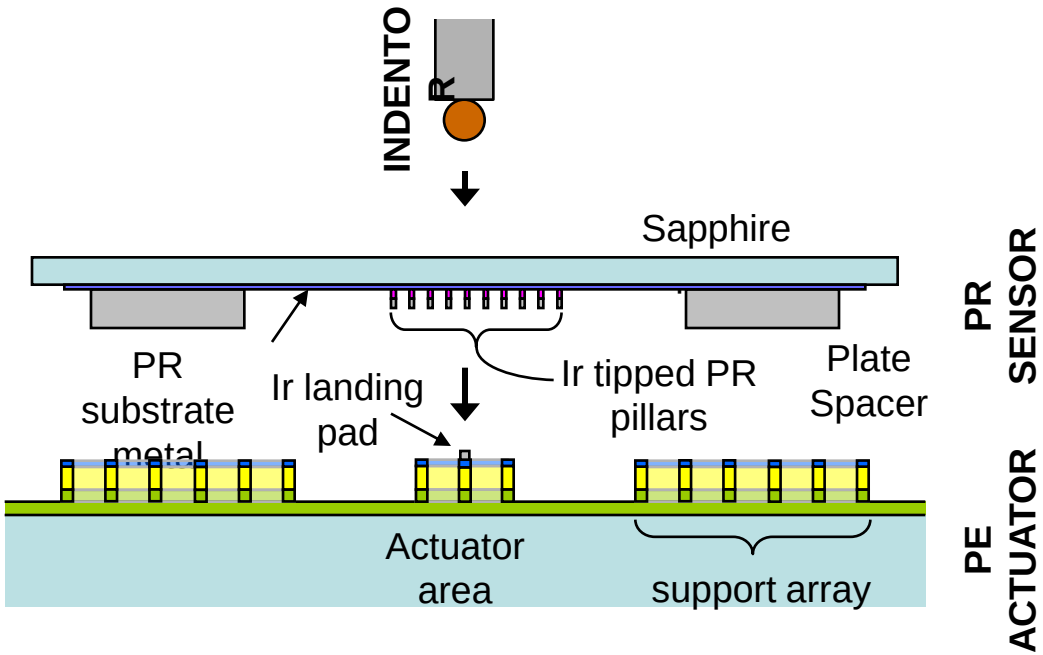
Device Test Structures

Materials

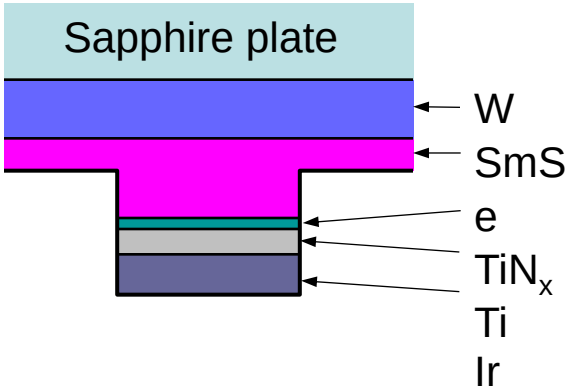
Goal: Demonstrate a fast, low-power device to take digital electronics beyond the voltage-scaling limits of the field-effect transistor.

Phase 1 | Phase 2 | Phase 3

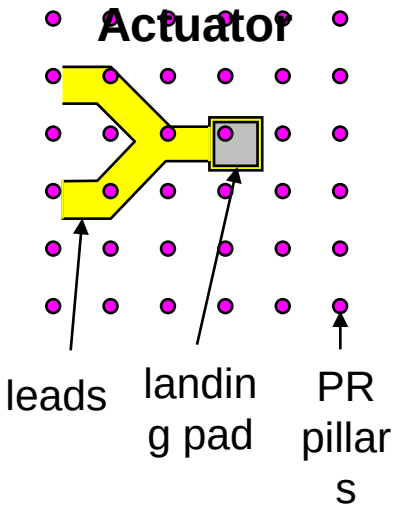
Split Actuator – Sensor Design for Gen-1 PET

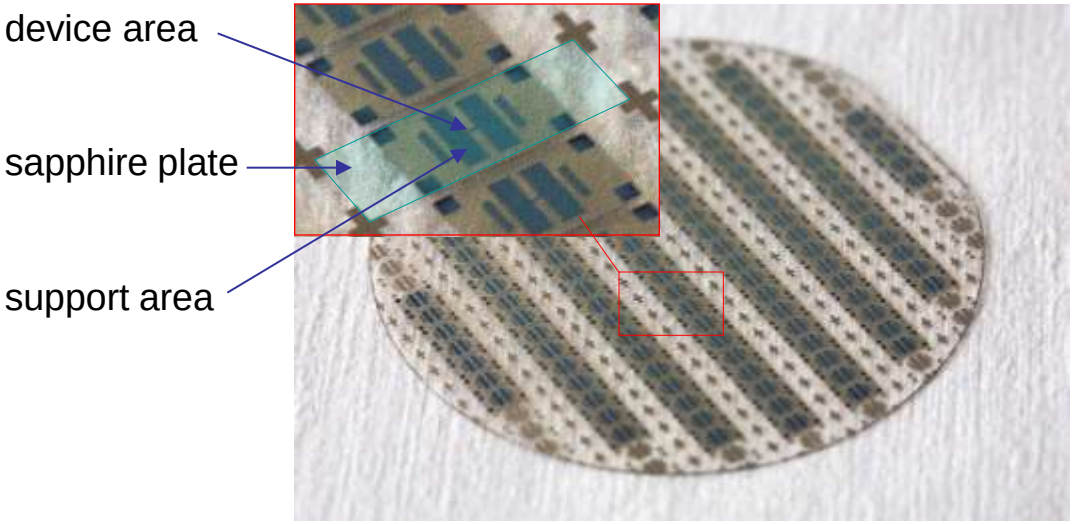


Sensor Pillar



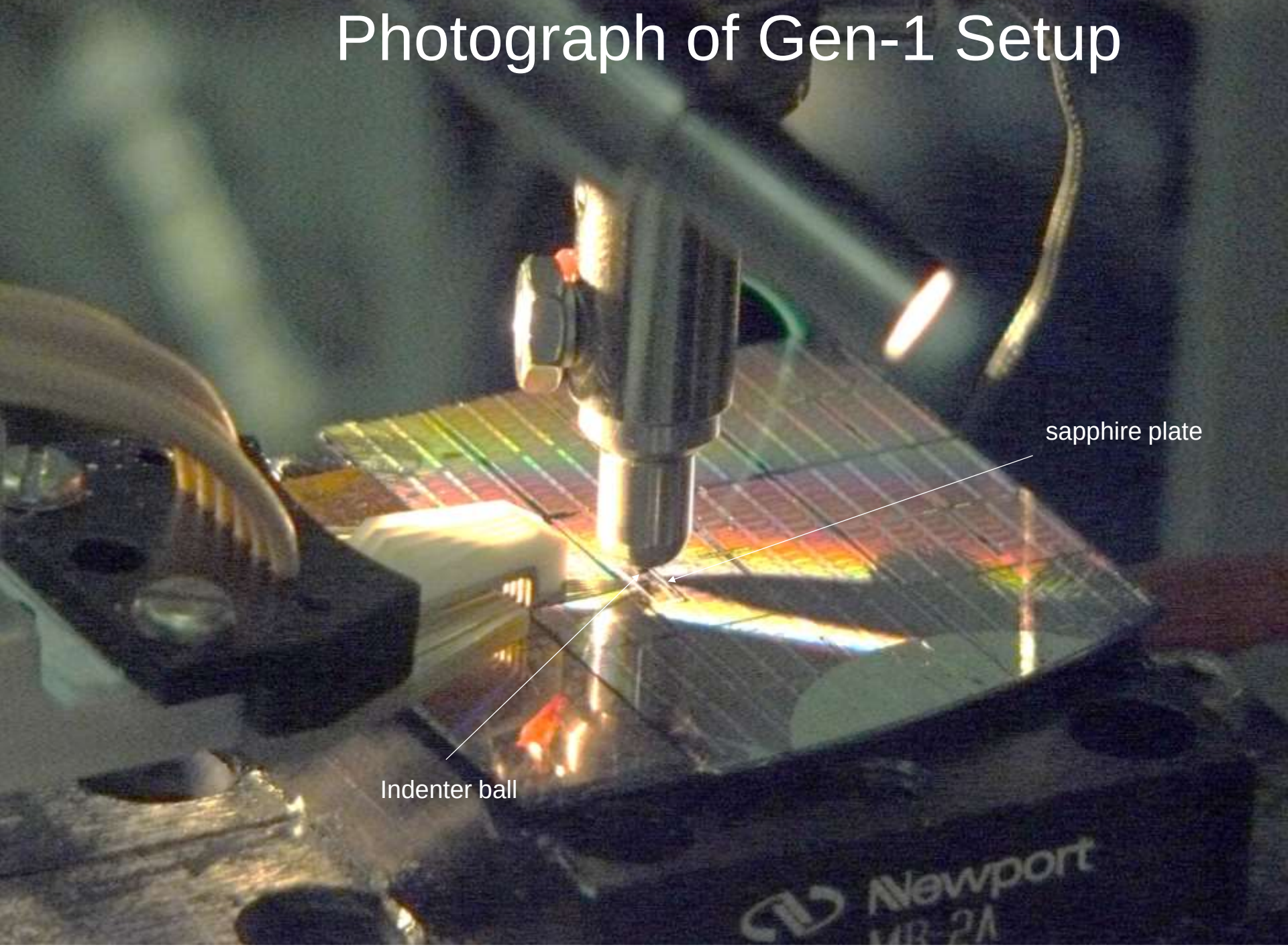
Pillars Randomly Aligned to Actuator



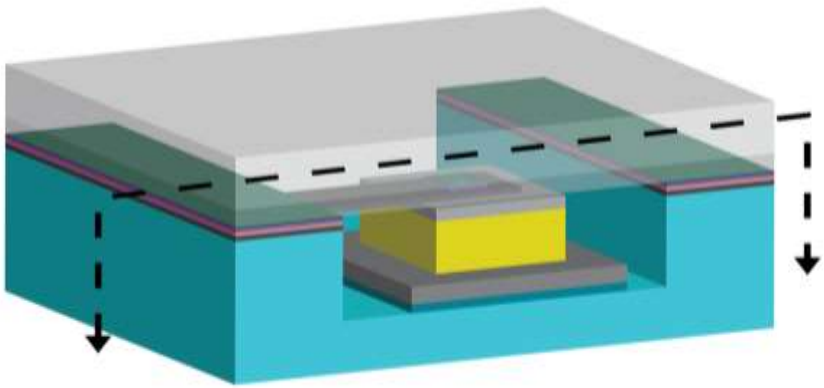


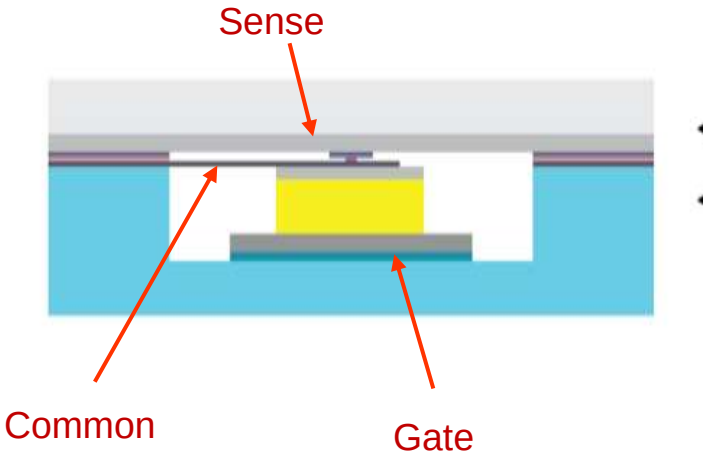
Processed Sapphire wafer

Photograph of Gen-1 Setup



Gen-2 PET Device





- **Engineering choice of process and materials relies heavily on Gen-1 learning.**
- **Preliminary experiments done to investigate compatibility issues.**

Possible Impediments to Scaling

PE

- Fundamental physics of relaxor piezos like PMN-PT – Theoretical research needed
- Practical limits on d_{33} at small scales ~ 30 nm – not known - Experimental research needed
- Dead layer at PE/metal boundary – controllable by materials

PR

- Minimum resistivity will limit RC time constant at small areas - OK for SmSe ultimate designs
- Minimum thickness ~ 3 nm - controlled by onset of tunneling – Needs experimental check
- Minimum width w, depends on lithography – sublithographic shapes possible
- Dead layer on surfaces (e.g. due to oxidation) or need for protective sidewall may limit the mechanical mobility of small PR pillars– test and explore solutions