Why Tunneling FETs Don't Work, and How to Fix Them

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A New Switch has to Satisfy Three Specifications

1. Steepness (or sensitivity)

   switches with only a few milli-volts

   60mV/decade $\Rightarrow$ **1mV/decade**

2. On/Off ratio. $10^6 : 1$

3. Current Density or Conductance Density

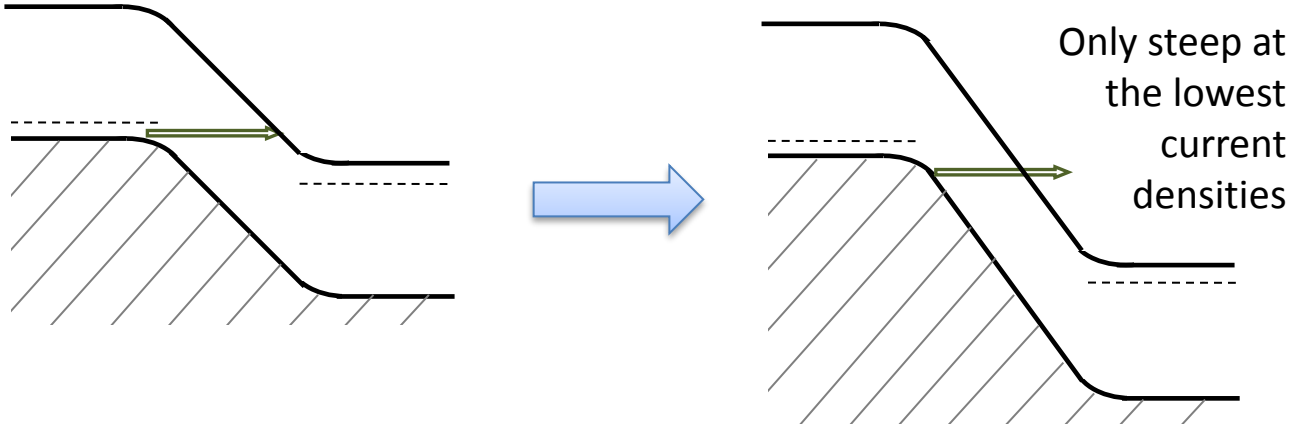
   (for miniaturization)

   old spec at 1Volt: 1 mAmp/micron

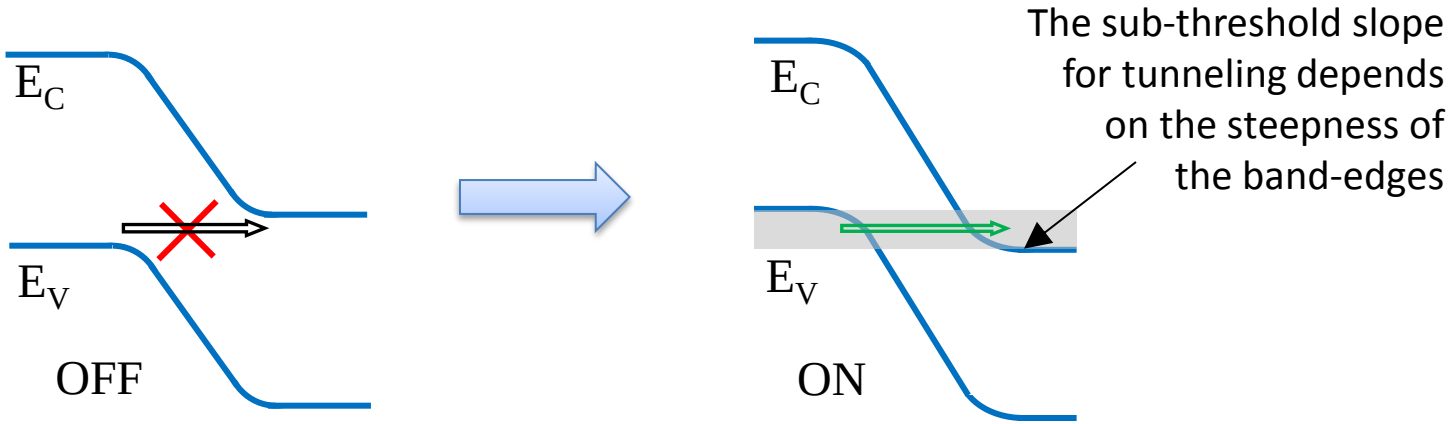
   our spec: **1 milli-Siemen/micron**

2 Ways to Obtain Steepness

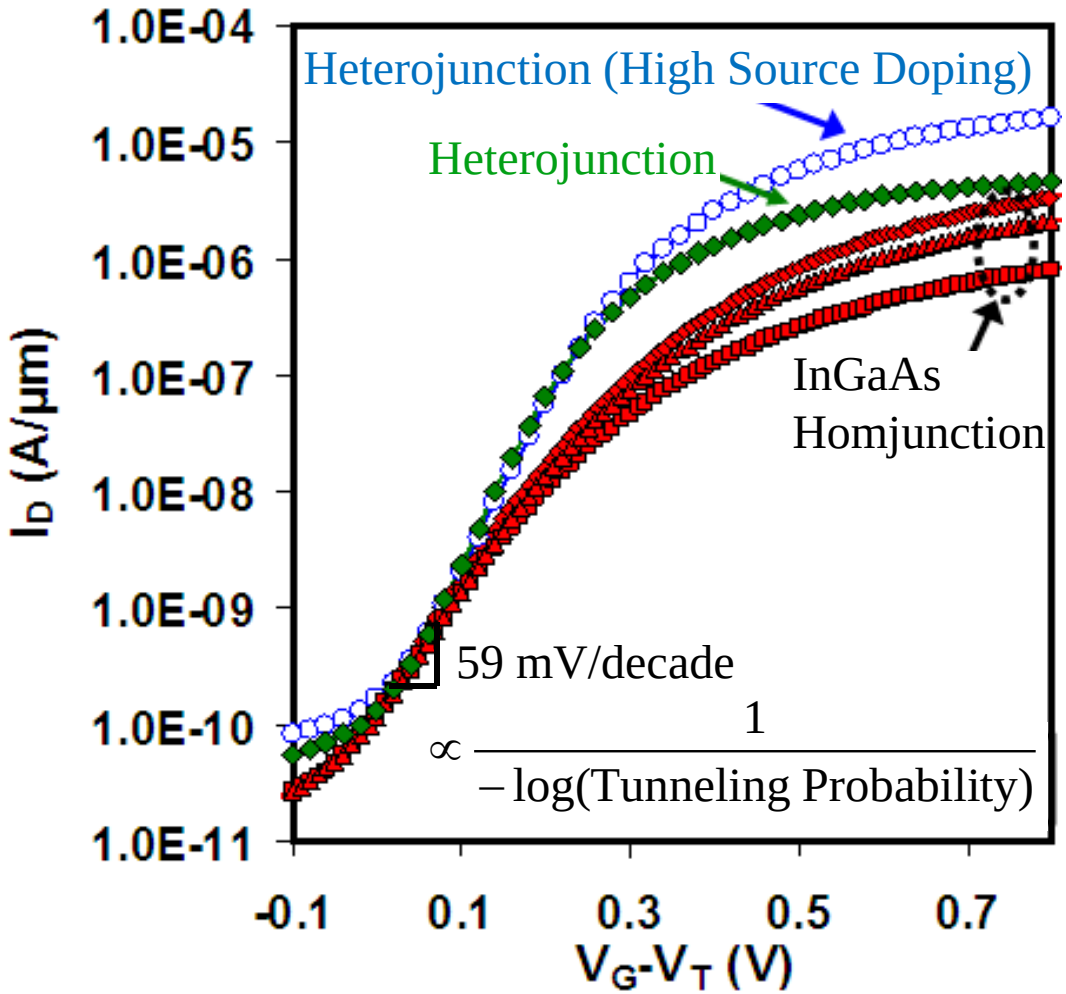
- **Modulate the Tunneling Barrier Thickness**



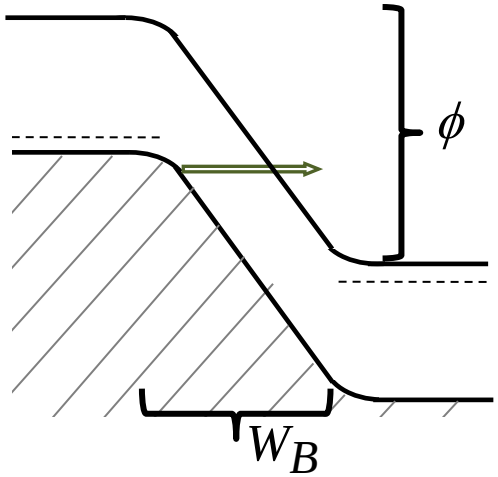
- **Energy Filtering - Density of States Switch**



Barrier Width Modulation Explains all Steep TFET Results and it's not Good Enough



G.Dewey, et all, *IEDM 2011* pp. 785-788, 2011



$$\text{Subthreshold Swing(SS)} \approx \frac{d\phi}{d\log(\text{T})}$$

$$\text{T} = \exp\left(\frac{-\alpha}{|\vec{F}|}\right) \qquad |\vec{F}| = \frac{\phi}{W_B}$$

$$SS \approx \left|\frac{1}{\log(T)} \times \frac{F}{dF(\phi)/d\phi}\right|$$

$$= \frac{\phi}{|\log(\text{T})|}$$

2 Ways to Obtain Steepness

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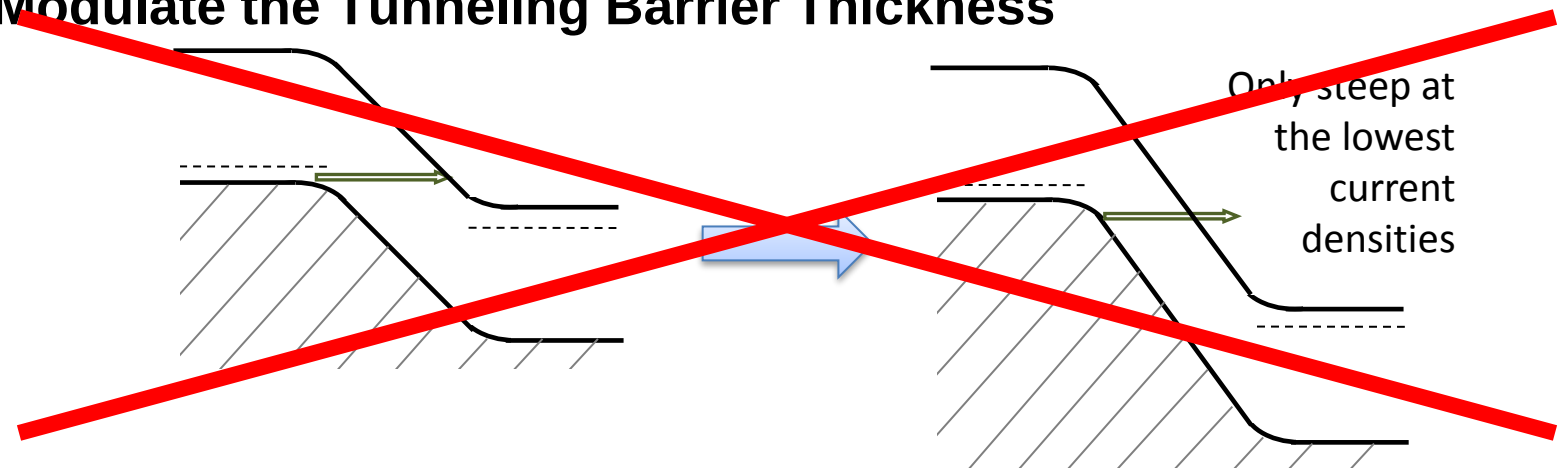
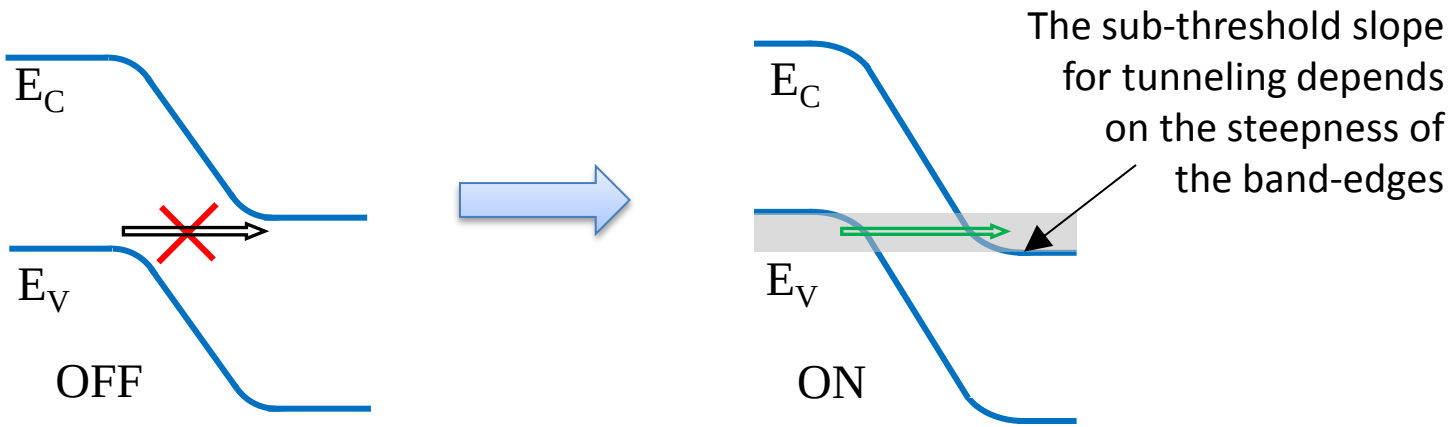
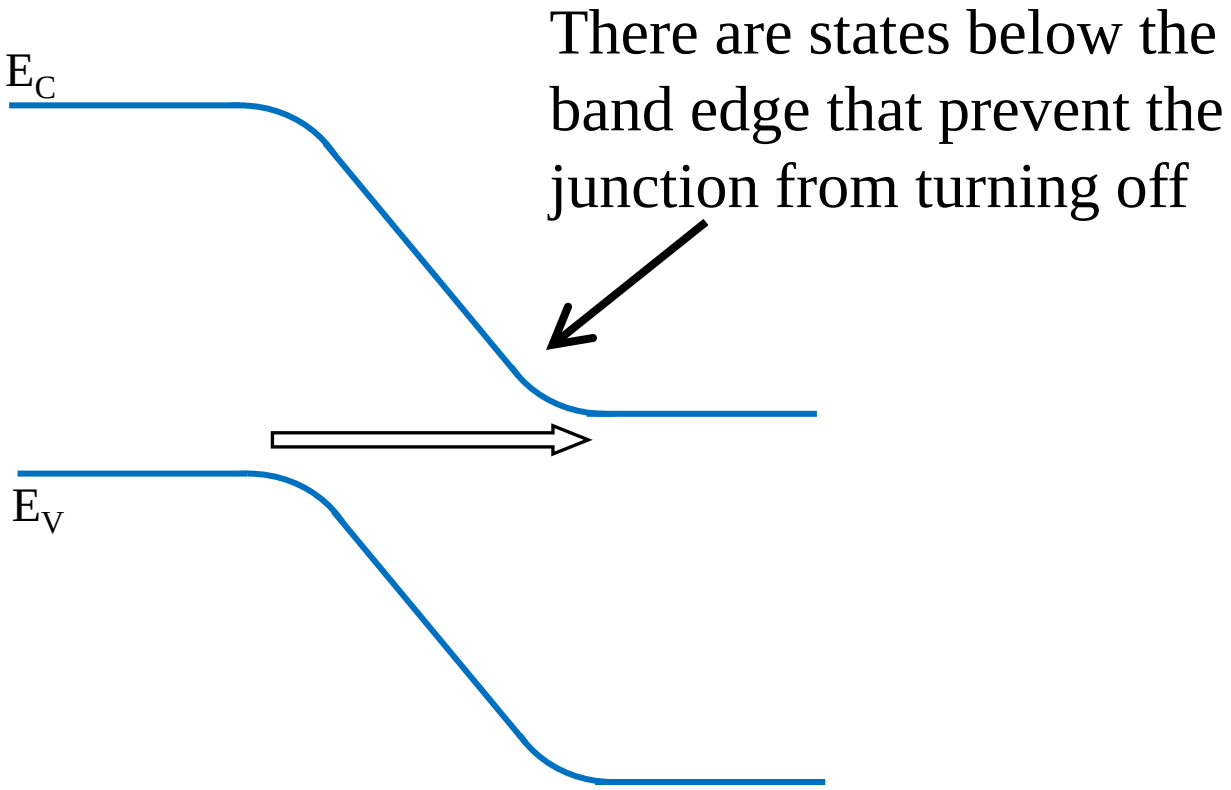


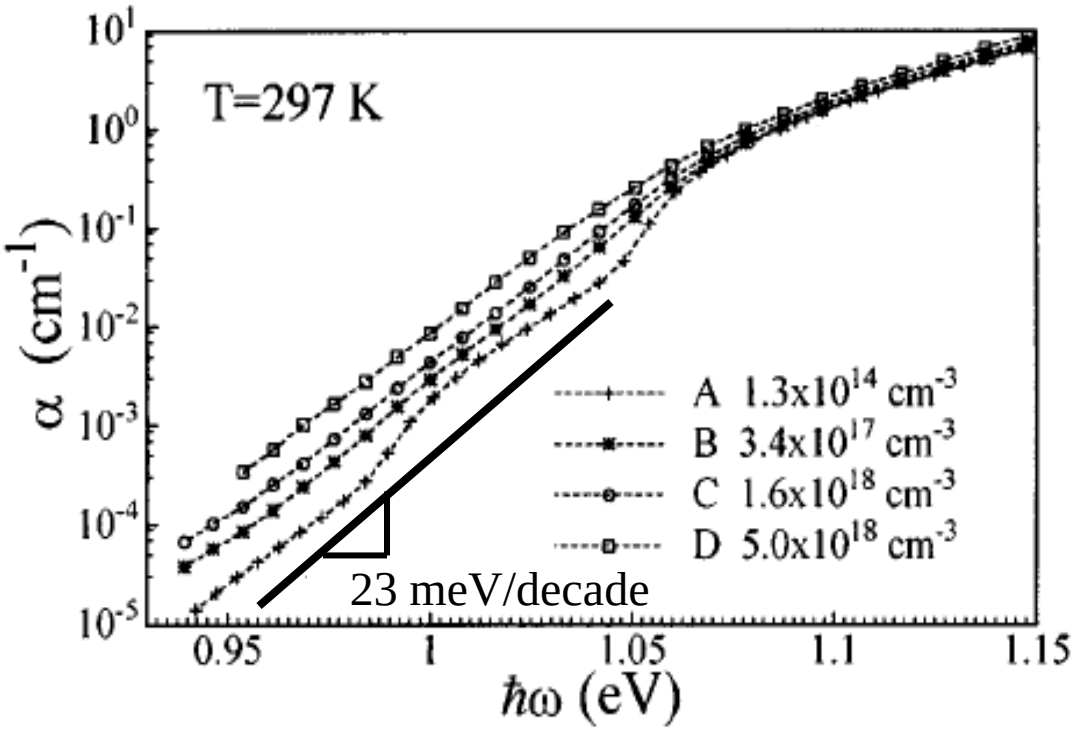
- **Energy Filtering Density of States Switch**



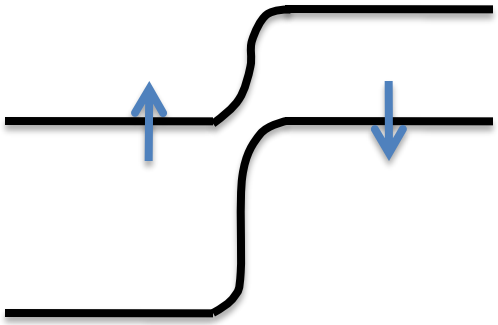
Band Tails Prevent a Steep Swing



Optical Absorption Shows a Steeper Edge than We've Ever Seen



The absorption curves of Silicon at different doping levels



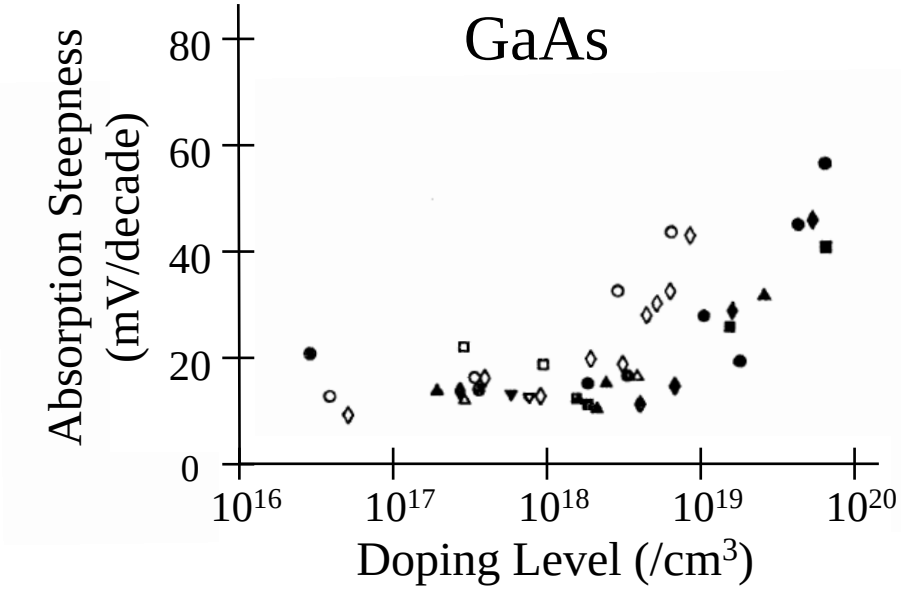
$\alpha(h\nu) \sim \exp\{(h\nu - E_g)/E_o\}$

$E_o \sim 10$meV for Silicon

~ 23 meV /decade

E. Daub and P. Wurfel, *Journal of Applied Physics,* vol. 80, pp. 5325-5331, 1996.

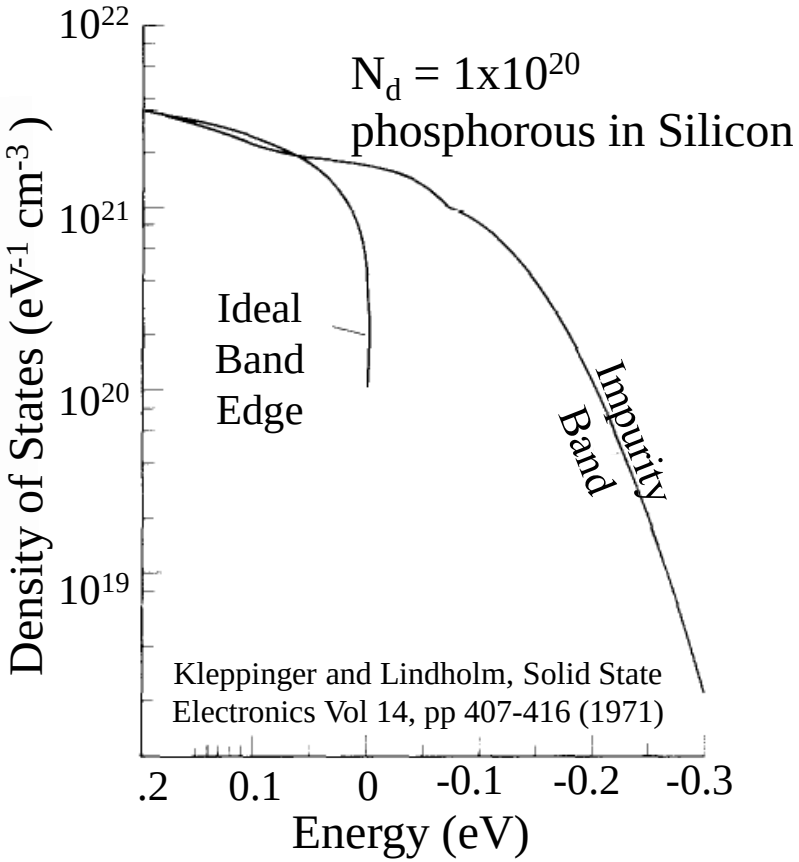
Optical Absorption Steepness Gets Worse With Doping



Undoped
~17 mV/decade

Heavily Doped
~ 60 mV/decade

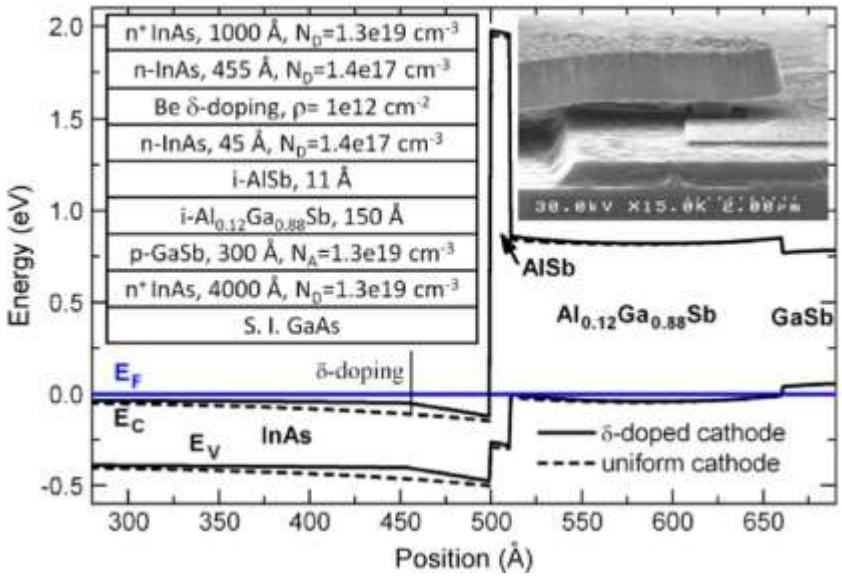
J. I. Pankove, "Absorption Edge of Impure Gallium Arsenide" *Physical Review*, vol 140 pp A2059-A2065, 1965

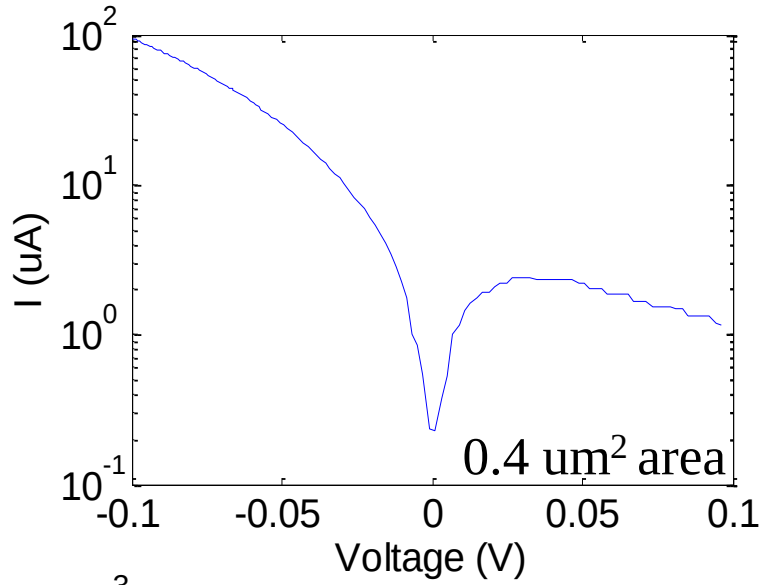


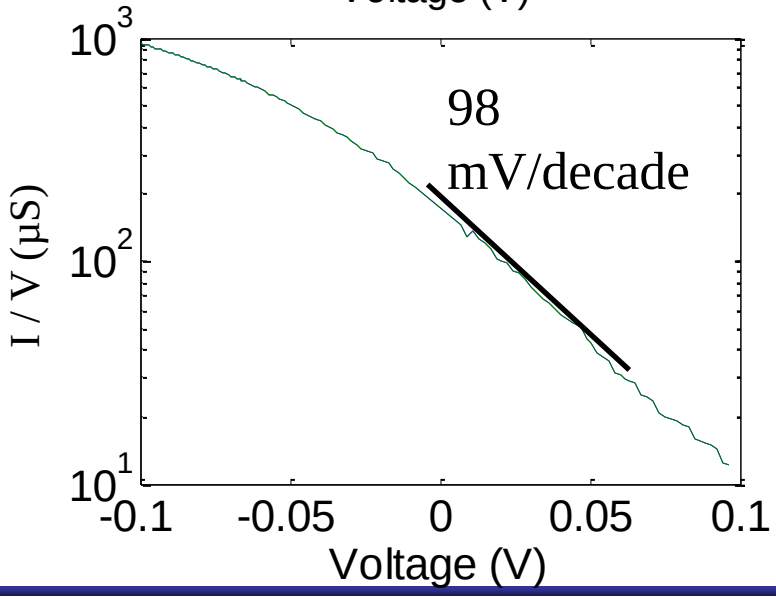
Doping induced potential variations are screened by free carriers. The slope will be far worse in a depletion region

Analyze the Diode Conductance to Measure Steepness

InAs / AlGaSb Backward Diode



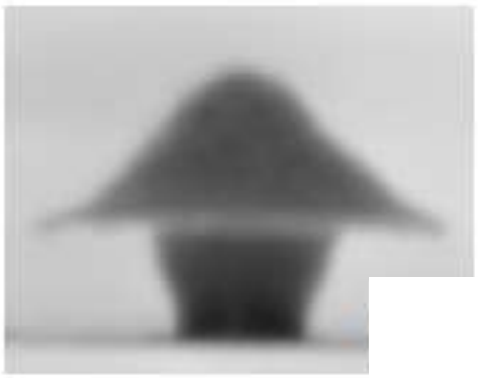


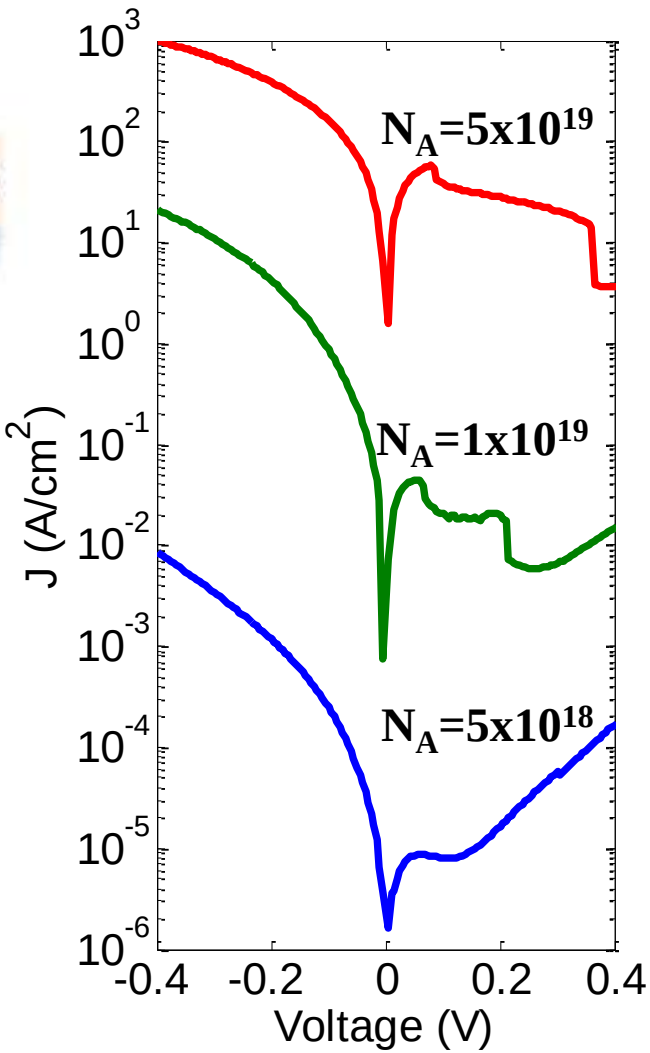


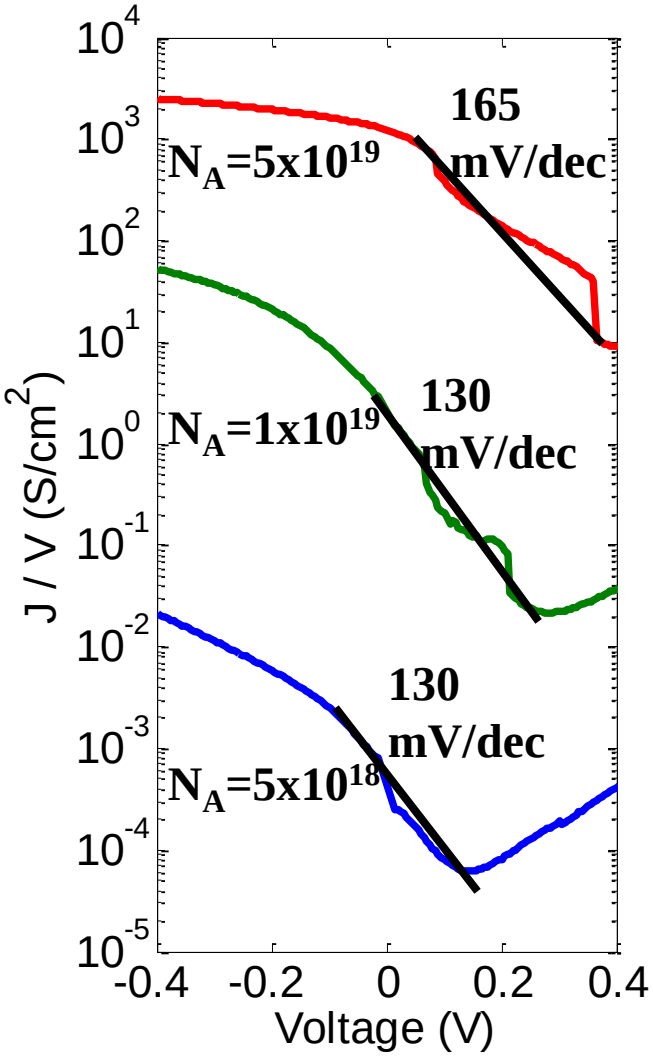
Zhang, Rajavel, Deelman, and Fay (2011)

GaAs Homojunction Diodes

$N_D=3x10^{19}$

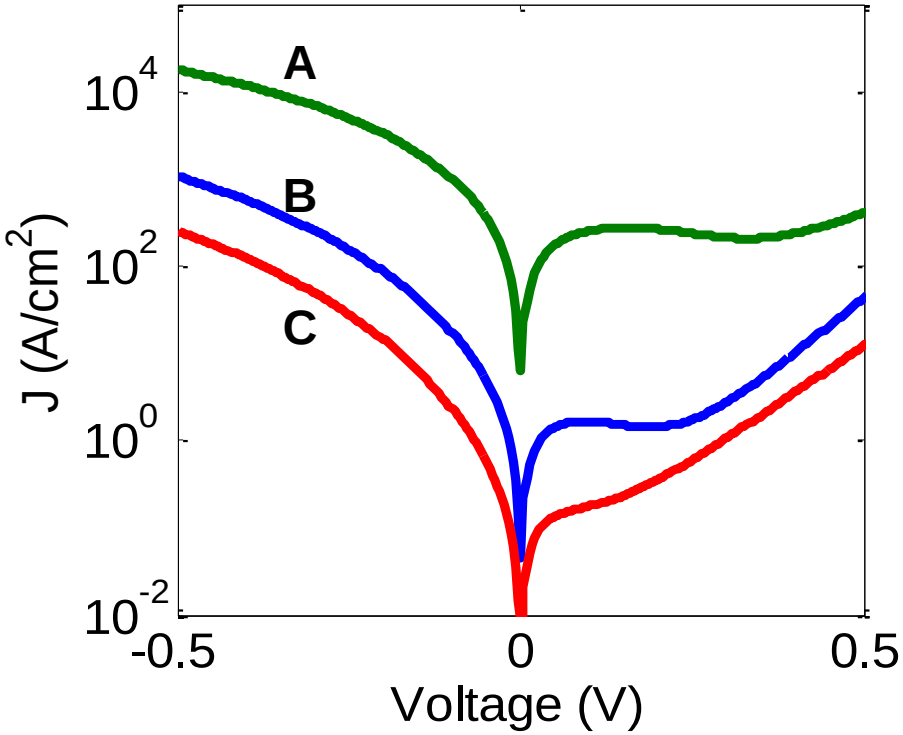


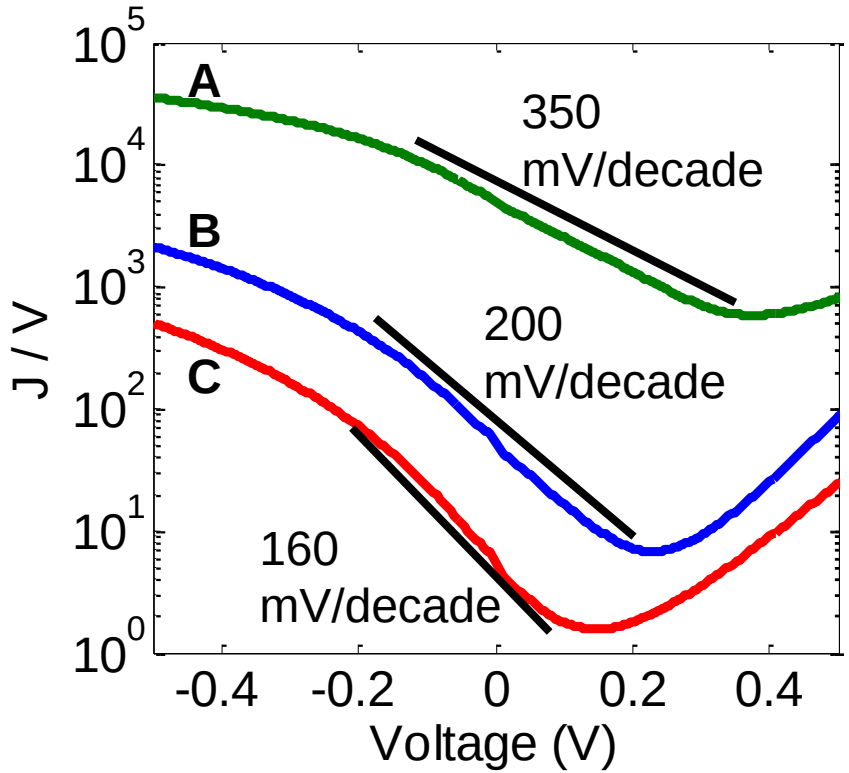


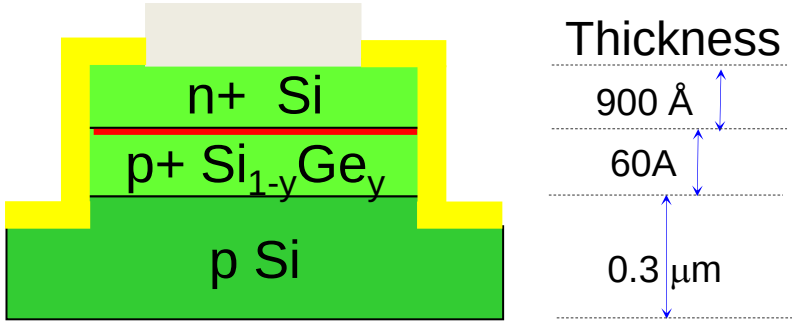


From Pawlik et all, "Benchmarking and Improving III-V Esaki Diode Performance with a Record 2.2 MA/cm2 Peak Current Density to Enhance TFET Drive Current" IEDM 2012, pp. 812-814

SiGe Epi Diodes Steeper at Lower Doping







(A) 5e19/3e20/3e19 n+/p+/p
(B) 1e19/1e20/3e19 n+/p+/p
(C) 1e19/1.5e20/1e17 n+/p+/p

Why so many Non-Steep Results?

Technological:

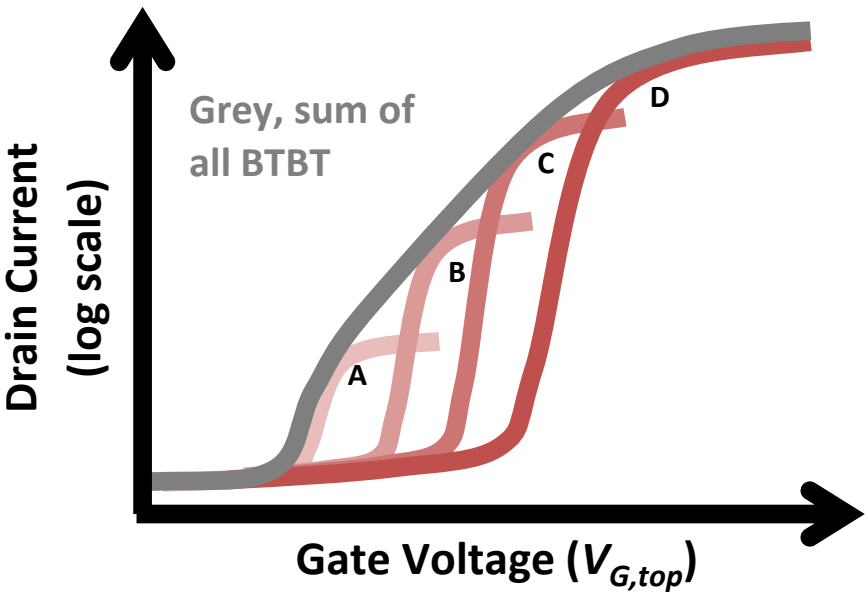
- **Band-tails caused by heavy doping**
- **Interface traps**
- **Mid-gap traps**
- **Electrostatic design (parasitic paths)**
- **Spatial Inhomogeneity of semiconductor--**
  - Doping & Thickness

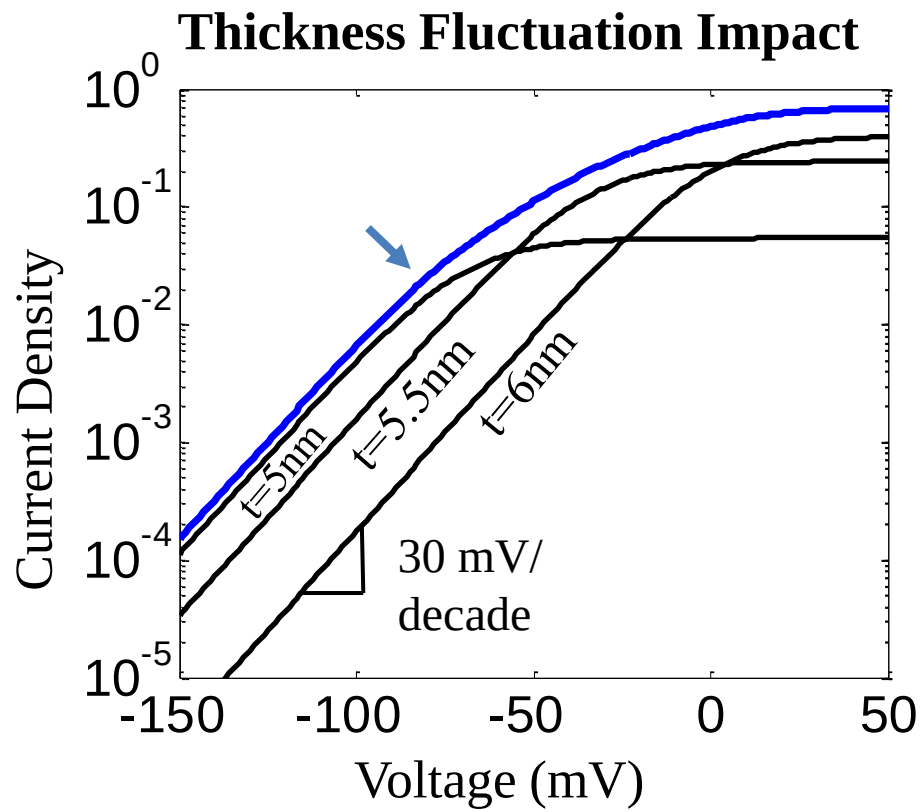
Fundamental

- Inherent band-tails
- Phonon effects
- Smearing quantized energy states in QW

Eliminate Spatial Inhomogeneity

- **Make the Devices Very Small.**
  - The threshold may not be reproducible, but so far the field doesn't have a single steep device.

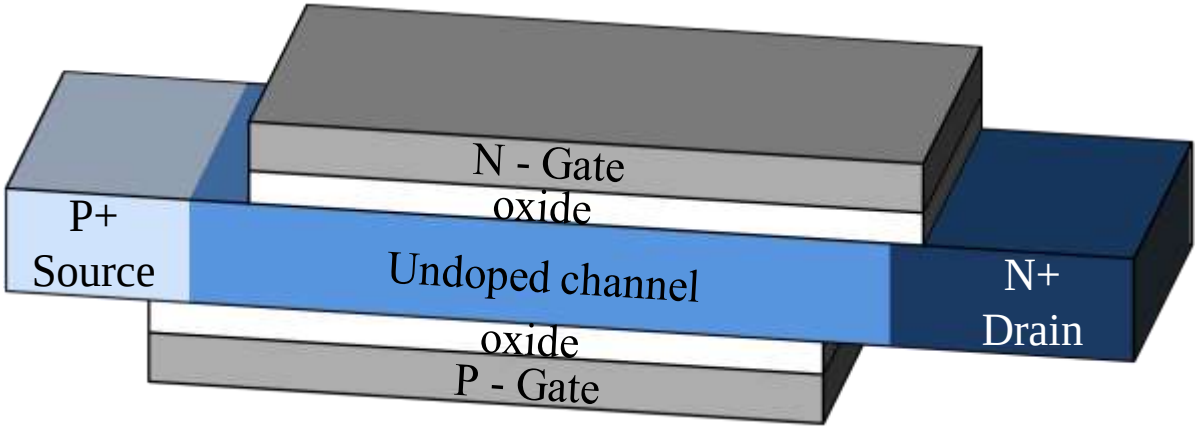


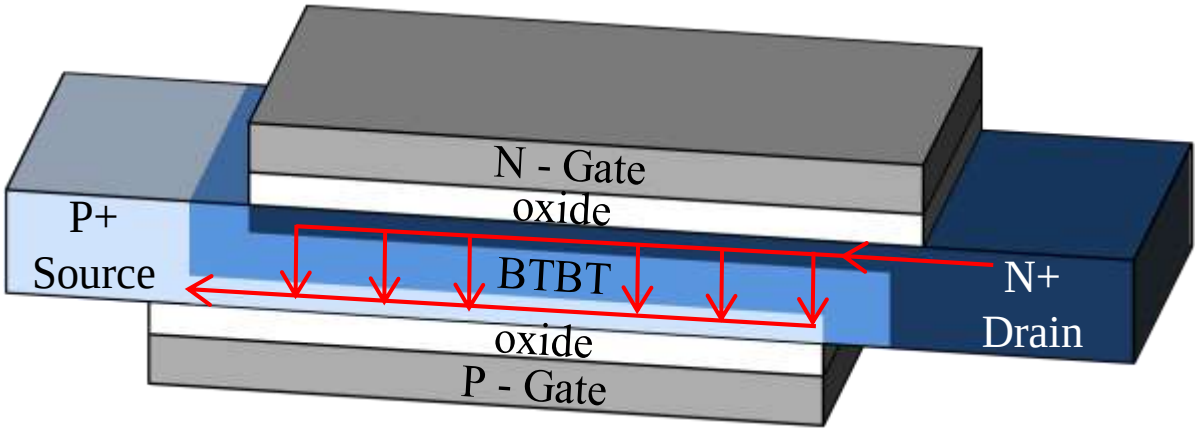


Eliminate Spatial Inhomogeneity Due to Doping

Bilayer TFET

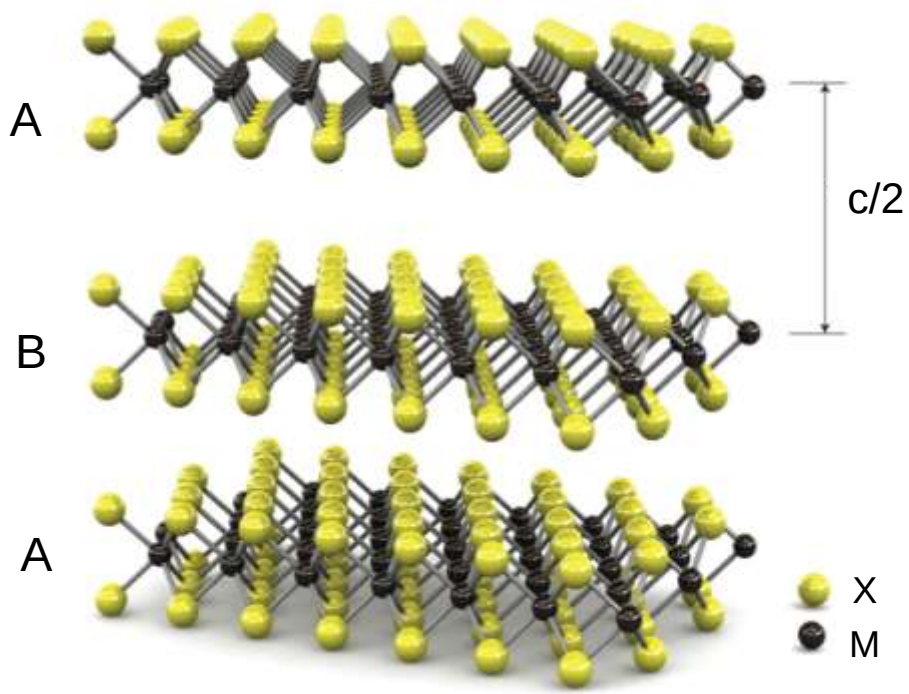
Replace doping with Work Function Control & Gate Control





For reproducible threshold voltage, thickness has to be atomically flat

Layered chalcogenides: atomic level flatness



- Scalable down to a single monolayer (~ 7 Angstroms)
- Lack dangling bonds; no native oxide
- van der Waals bonding/interfaces
- Uniform thickness – sharp band edges

A New Switch has to Satisfy Three Specifications

1. Steepness (or sensitivity)

   switches with only a few milli-volts

   60mV/decade $\Rightarrow$ **1mV/decade**

2. On/Off ratio. $10^6 : 1$

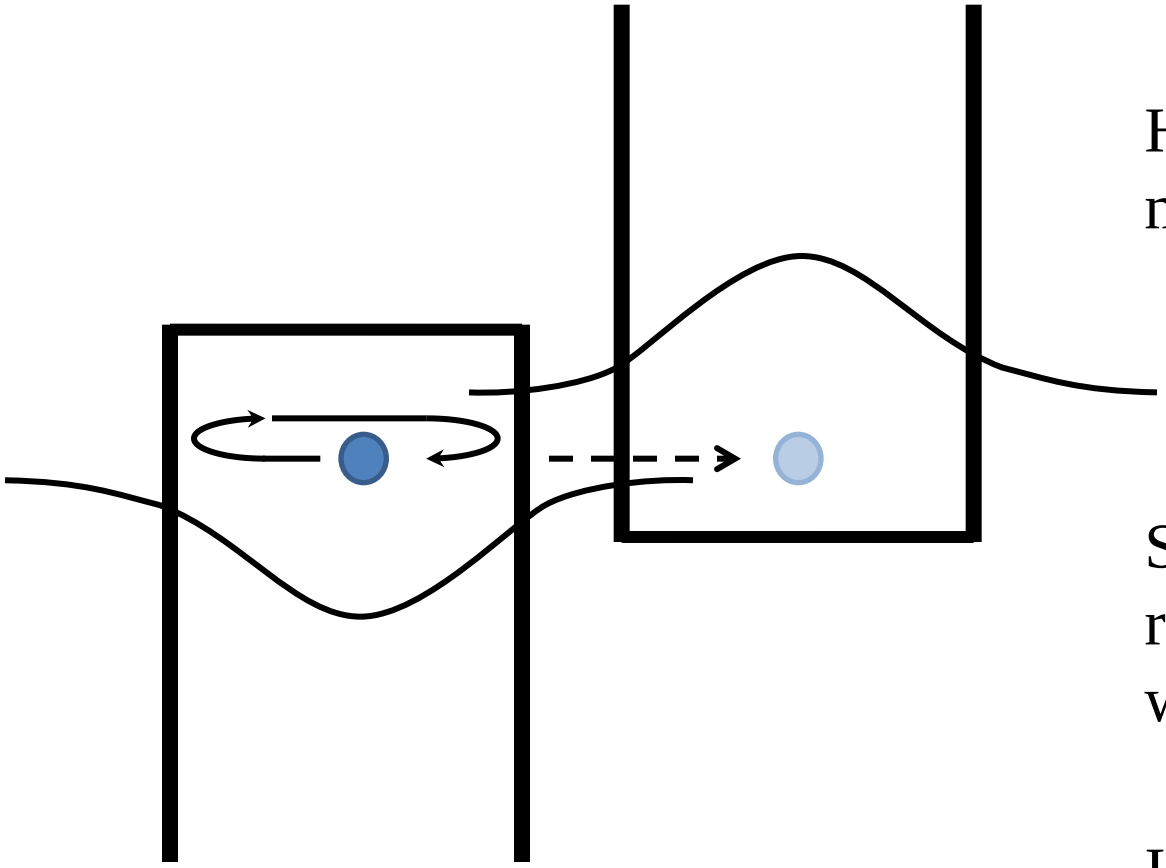
3. Current Density or Conductance Density

   (for miniaturization)

   old spec at 1Volt: 1 mAmp/micron

   our spec: **1 milli-Siemen/micron**

Confinement in the Tunneling Direction Increases Conductance



Higher energy results in more tunneling attempts

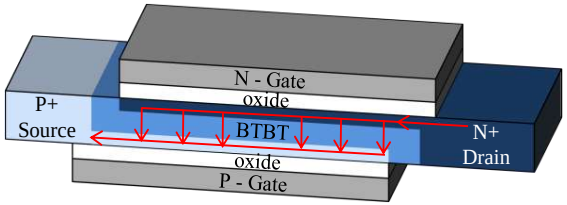
Smaller quantum well results in a larger wavefunction overlap

Increase Conductance by 10-100X

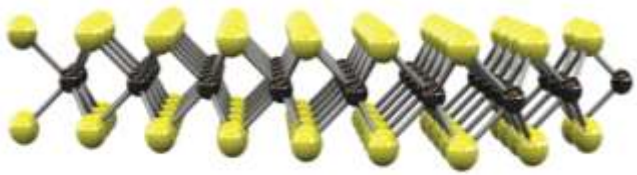
$$E_z = \frac{1}{2} m v_z^2$$

Summary

- **We have not yet figured out how to make a single steep device at high I_{ON}**
- **We must get beyond thickness modulation and use energy filtering**
  - **Need a sharp band edge**
- **Use small devices to eliminate spatial inhomogeneity**
- **Eliminate doping inhomogeneity**
  - **Use work functions to get carriers**



- **Use Molecular Control for uniform reproducible thresholds**



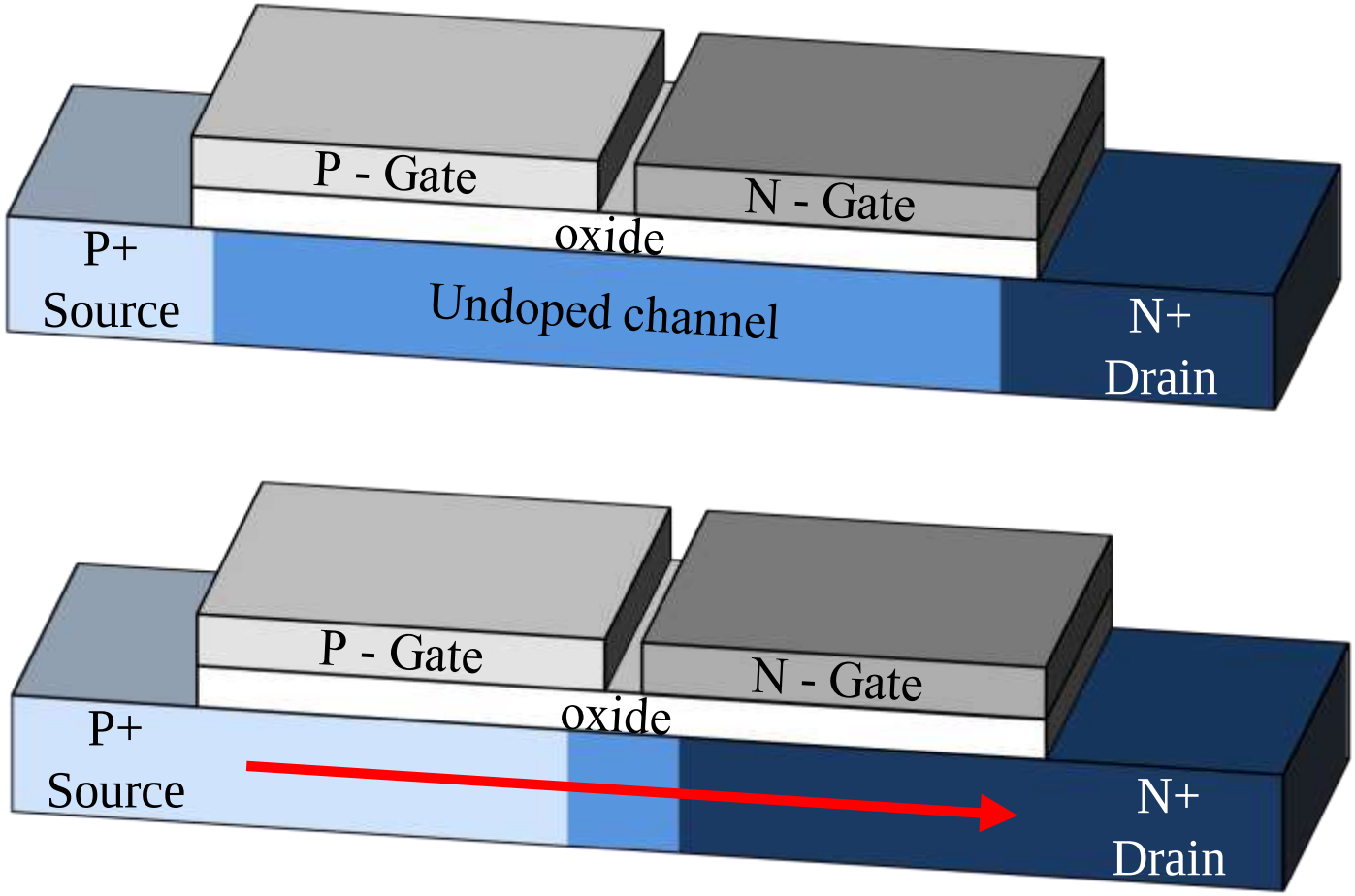
chalcogenide monolayers

Questions?

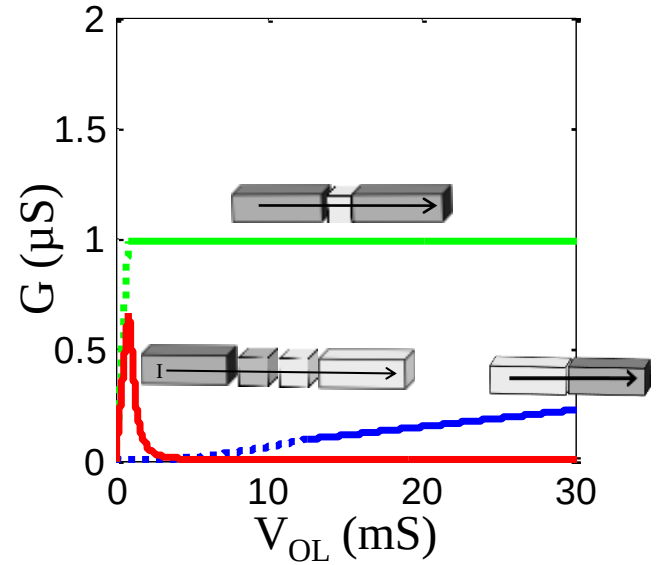
Extra Slides

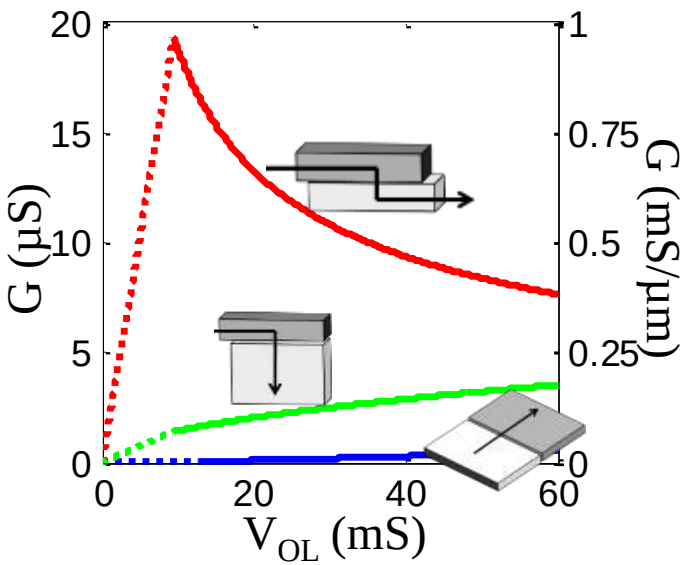
How to Eliminate Doping

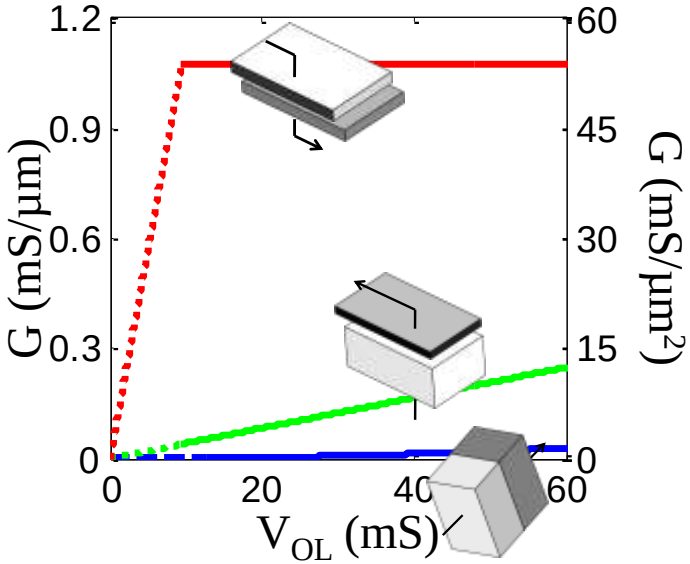
Lateral Double Gate TFET



Compare Confined Structures



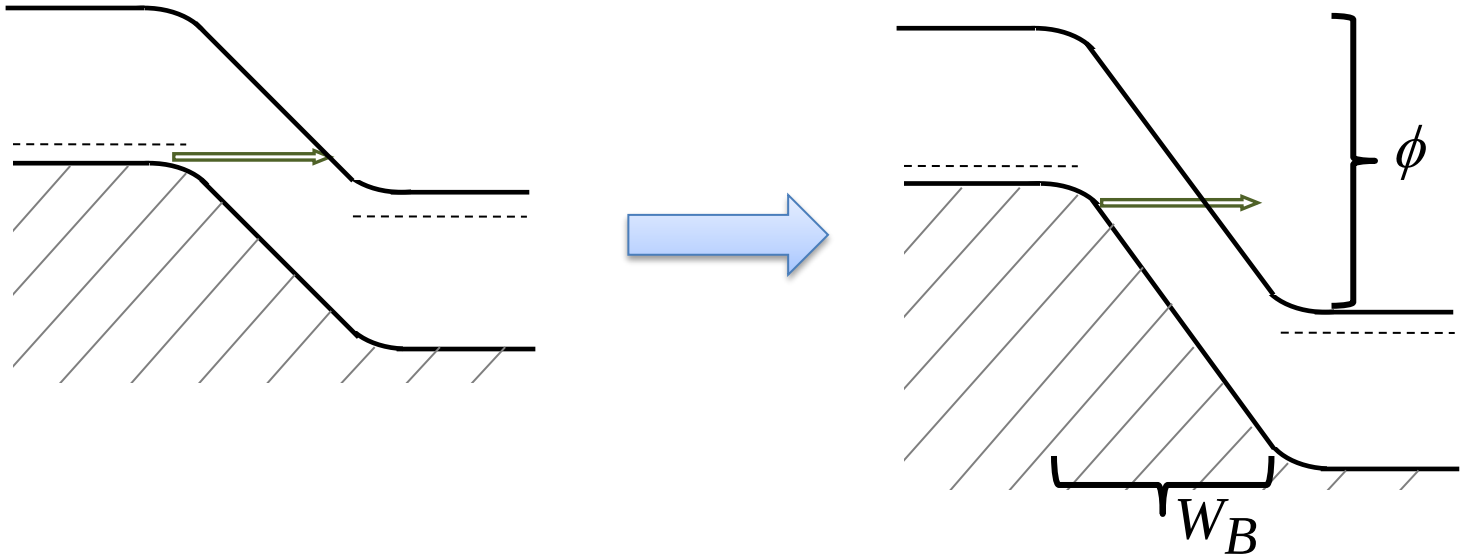




T=1%, $m^*=0.1m_e$
Overlap Lengths=20 nm
Confinement Energies=130 meV

Conductance increase verified by NEGF

Find the Subthreshold Swing Due to Barrier Width Modulation



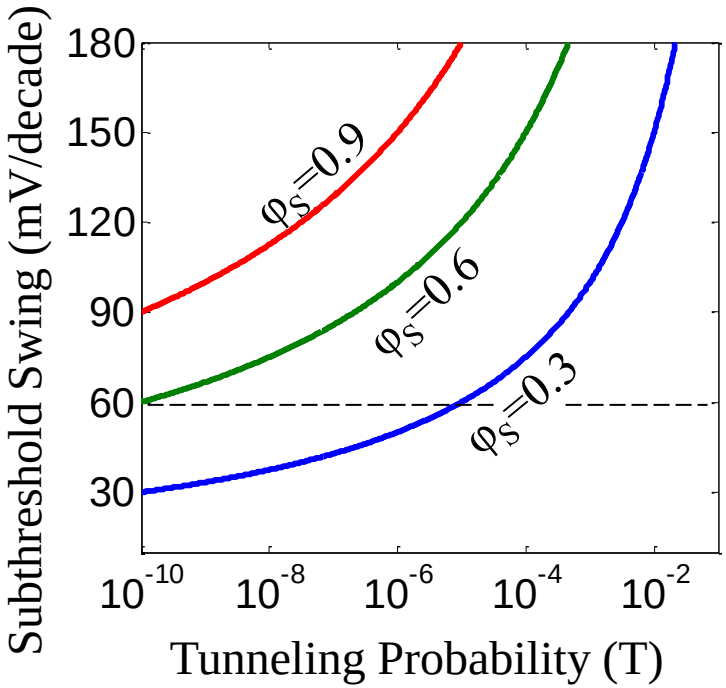
$$S_{tunnel} \approx \frac{d\phi}{d\log(\mathrm{T})} \quad \text{Use} \quad \mathrm{T} = \exp\left(\frac{-\alpha}{|\vec{F}|}\right) \quad \text{and} \quad \left|\vec{F}\right| = \frac{\phi}{W_B}$$

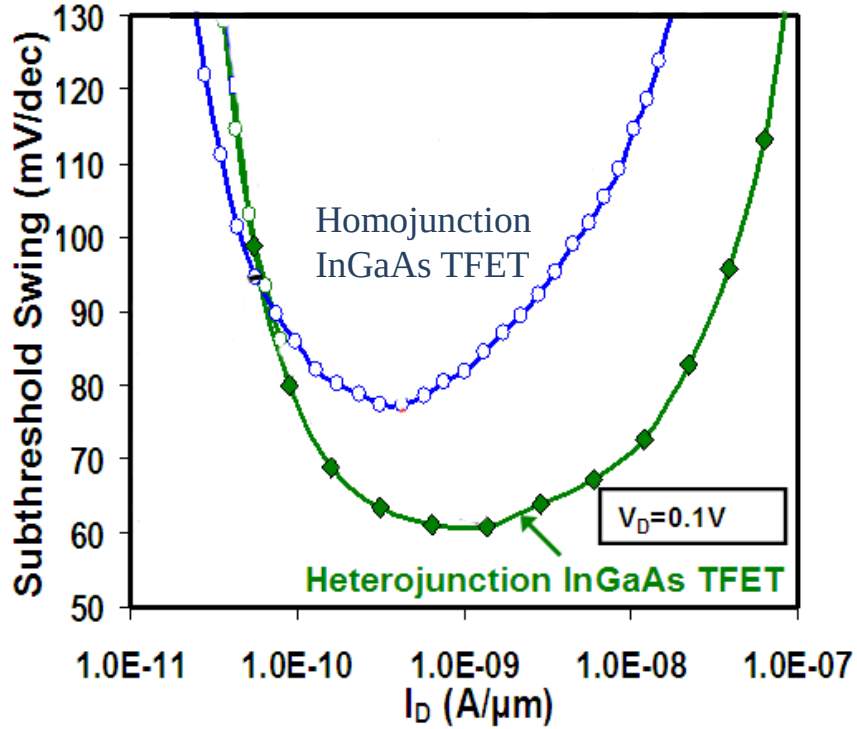
$$\boxed{S_{tunnel} \approx \left|\frac{1}{\log(T)} \times \frac{F}{dF(\phi)/d\phi}\right| = \frac{\phi}{|\log(\mathrm{T})|}}$$

T = Tunneling Probability

Barrier Width Modulation Explains all Steep TFET Results and it's not Good Enough

$$S_{tunnel} \approx \left| \frac{\phi}{\log(T)} \right|$$





G. Dewey, et all, *2011 IEEE International Electron Devices Meeting* (IEDM 2011), p. 33.6, 2011

Can we use $S_{Btunnel}$?

$$S_{tunnel} \approx \left| \frac{\phi}{\log(T)} \right|$$

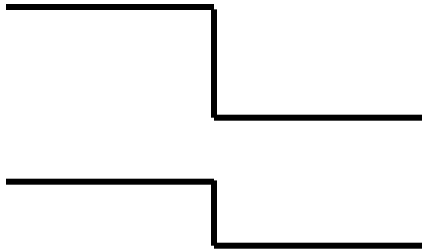
Consider T~ 1%

Log(T) = -2

For S_{tunnel} = 60 mV/decade, need φ of 120 meV

Is this reasonable?

$\log(I_{ON}/I_{OFF}) = 120 \text{ meV} / S_{DOS}$



For 5 orders of magnitude on/off need S_{DOS} < 24 mV/decade

Use steep S_{DOS} for steep subthreshold swing

Find S_{tunnel}

$$S_{tunnel} \approx \frac{d\phi_s}{d\log(T)}$$

$$T(\vec{F}) = \exp\left(\frac{-\pi(m^*_{tunnel})^{1/2} E_g^{3/2}}{2\sqrt{2}\hbar q\,|\vec{F}|}\right) = \exp\left(\frac{-\alpha}{|\vec{F}|}\right)$$

$$S_{tunnel} \approx \left(\log(e)\times\alpha\times\frac{1}{\left|\vec{F}\right|^2}\times\frac{d\vec{F}(\phi_s)}{d\phi_s}\right)^{-1}$$

use $\left|\vec{F}\right| = -\dfrac{\log(e)\times\alpha}{\log(T)}$

$$S_{tunnel} \approx \left|\frac{1}{\log(T)}\times\frac{F}{d\vec{F}(\phi_s)/d\phi_s}\right|$$

Lateral/point TFET

$$\left|\vec{F}\right| = \frac{\phi_s}{l_{screening}}$$

$$\frac{\left|\vec{F}\right|}{dF/d\phi_s} = \phi_s$$

Bilayer TFET

$$\left|\vec{F}\right| = \frac{\phi_s}{t_{body}}$$

$$\frac{\left|\vec{F}\right|}{dF/d\phi_s} = \phi_s$$

$$\boxed{S_{tunnel} \approx \left|\frac{\phi_s}{\log(T)}\right|}$$

Find $S_{Barrier}$

Vertical TFET

$$\left|\vec{F}\right| = \frac{\phi_s}{W_{depletion}} \frac{= \phi_s}{\sqrt{\varepsilon_s \phi_s / 2qN_d}}$$

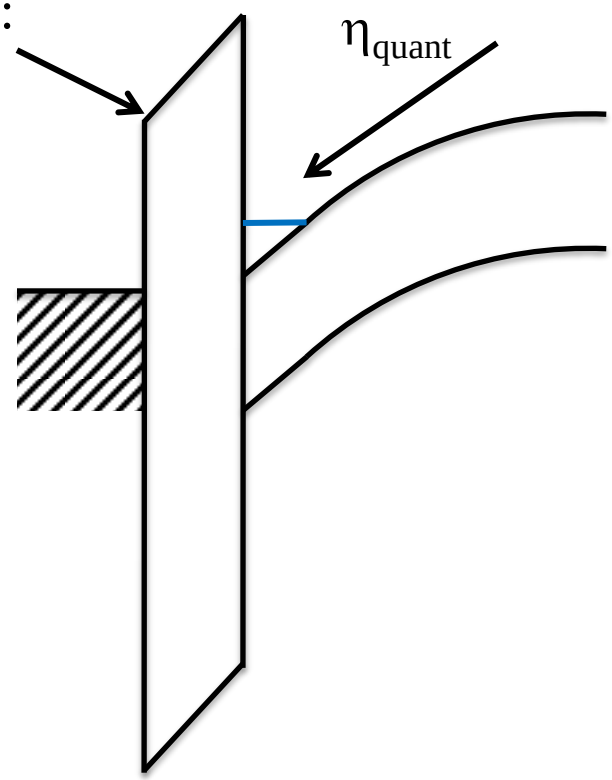
$$\frac{d\vec{F}}{\phi_s} = \frac{1}{2}\sqrt{\frac{2qN_d}{\varepsilon_s}}\phi_s^{-1/2} = \frac{1}{2\phi_s}\vec{F}$$

$$S_{tunnel} \approx \left|\frac{2 \times \phi_s}{\log(T)}\right|$$

Need to Maximize Gate Efficiency

Voltage lost on the gate oxide: η_{el}

Triangular barrier gets steeper, which increases the confinement energy: η_{quant}



$$\eta_{gate} = \eta_{el} \times \eta_{quant}$$

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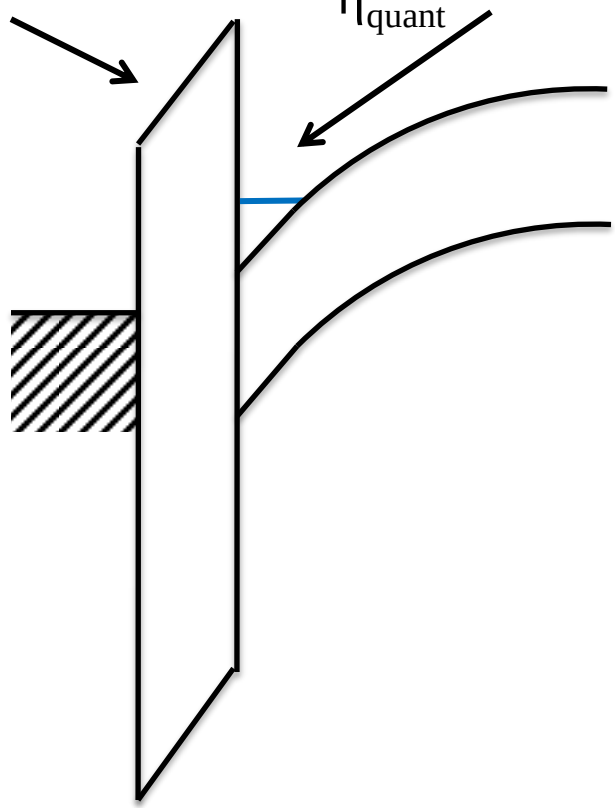
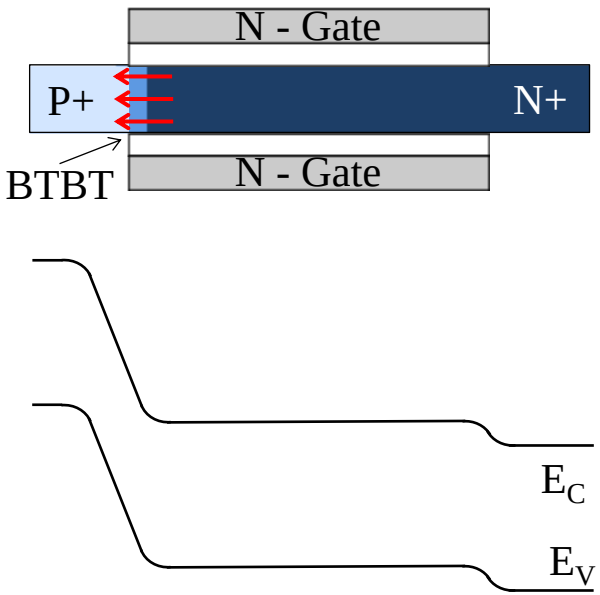
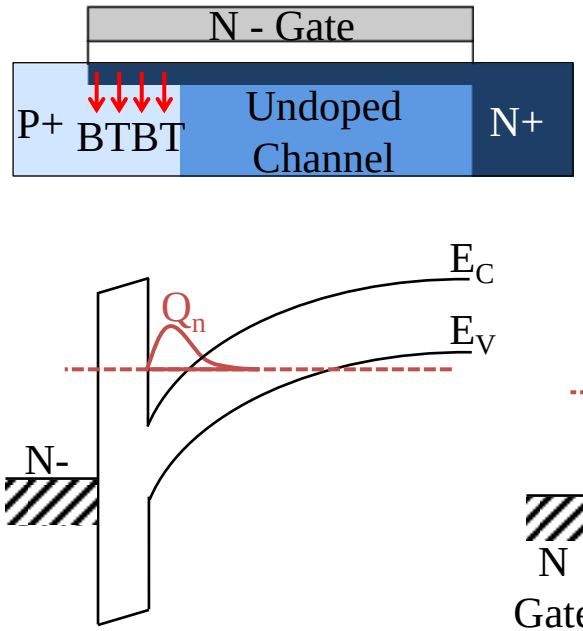
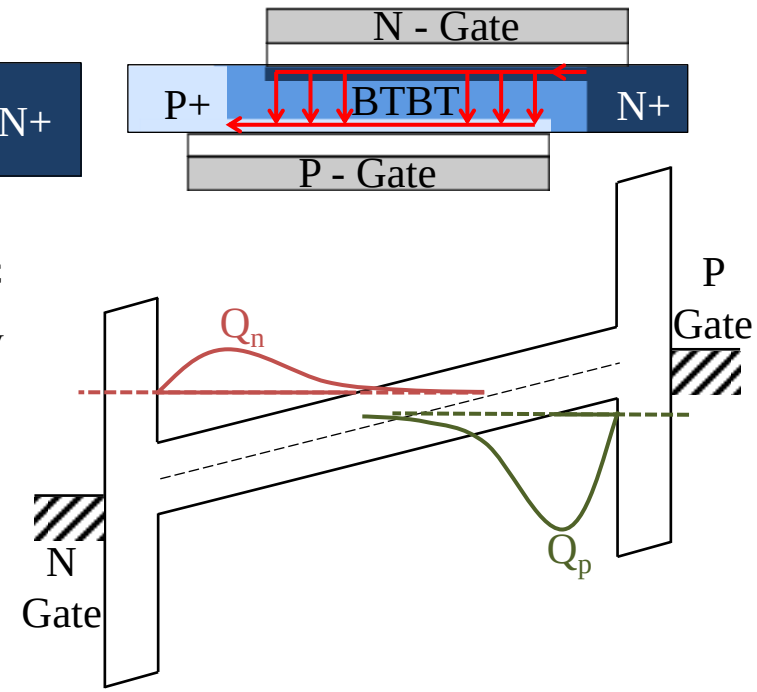


$$\eta_{gate} = \eta_{el} \times \eta_{quant}$$

Compare Different Geometries







FinFet Electrostatics
$\rightarrow \eta_{el} \sim 100\%$

Quantization Set by Geometry
$\rightarrow \eta_{quant} \sim 100\%$

$\eta_{quant} \times \eta_{el} \sim 100\%$

Planar FET Electrostatics
$\rightarrow \eta_{el} \sim 80\text{-}90\%$

Confined Electrons
$\rightarrow \eta_{quant} \sim 80\text{-}90\%$

$\eta_{quant} \times \eta_{el} \sim 70\text{-}80\%$

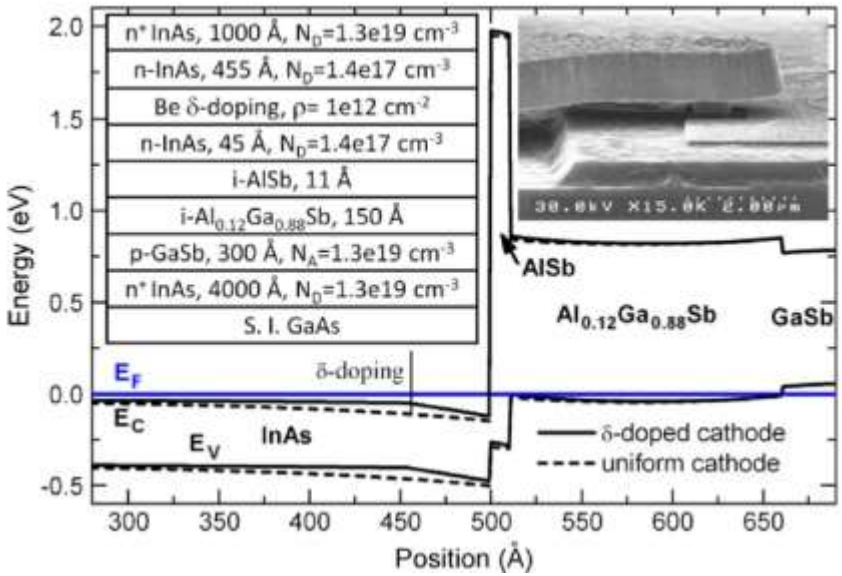
Two gate oxides and thin body
$\rightarrow \eta_{el} \sim 60\text{-}70\%$

Confined Electrons and Holes
$\rightarrow \eta_{quant} \sim 60\text{-}70\%$

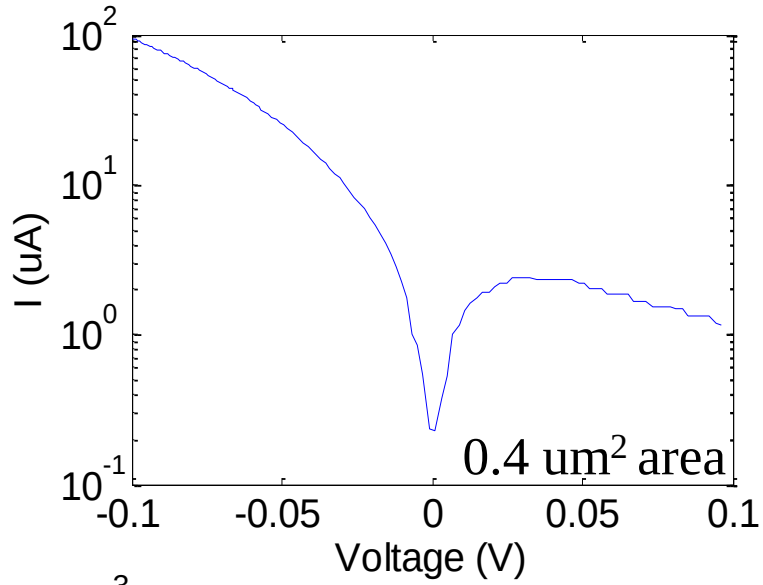
$\eta_{quant} \times \eta_{el} \sim 40\text{-}50\%$

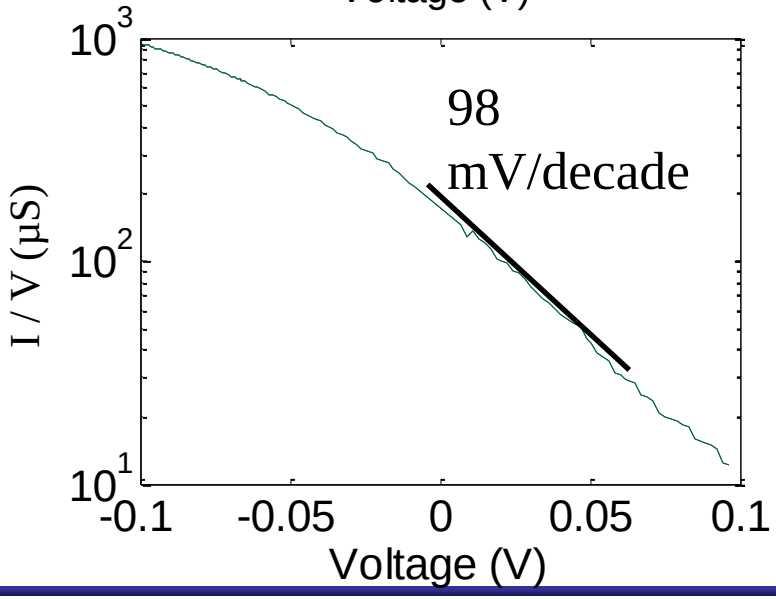
Analyze the Diode Conductance to Measure Steepness

InAs / AlGaSb Backward Diode

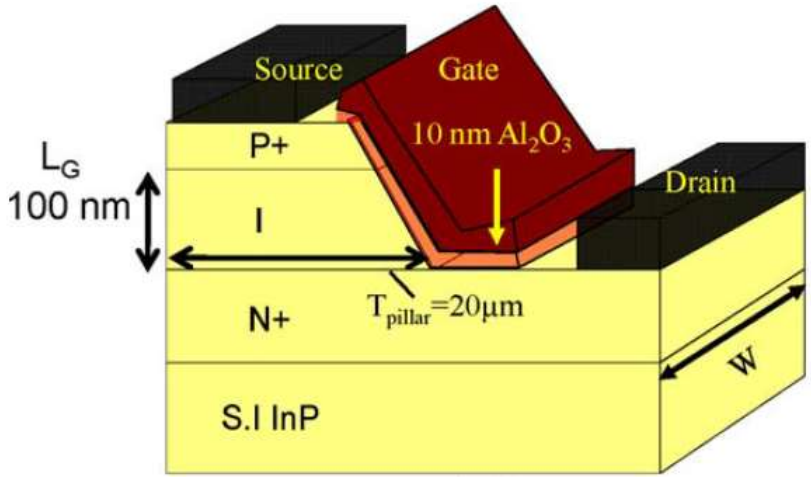


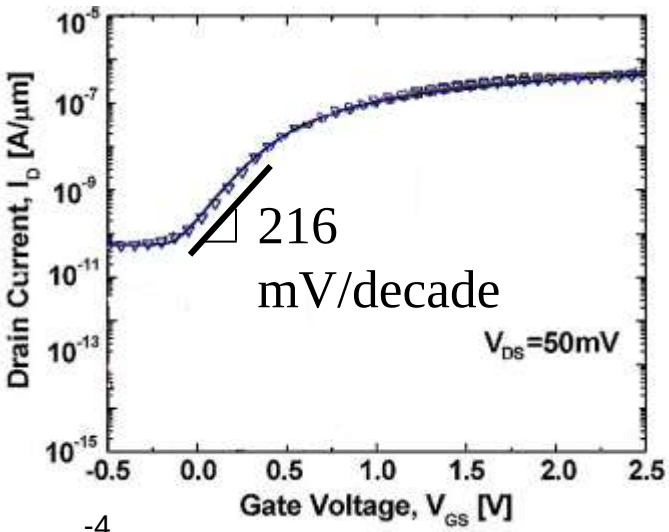
Zhang, Rajavel, Deelman, and Fay (2011)

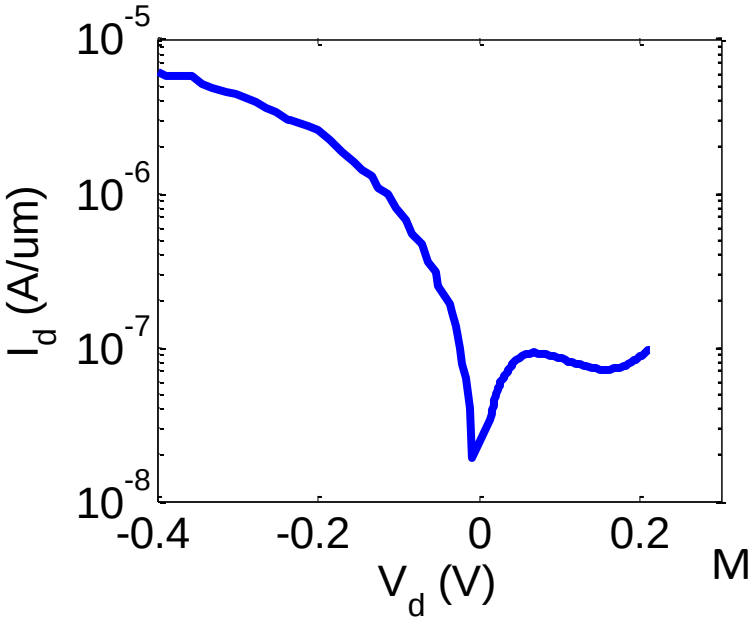


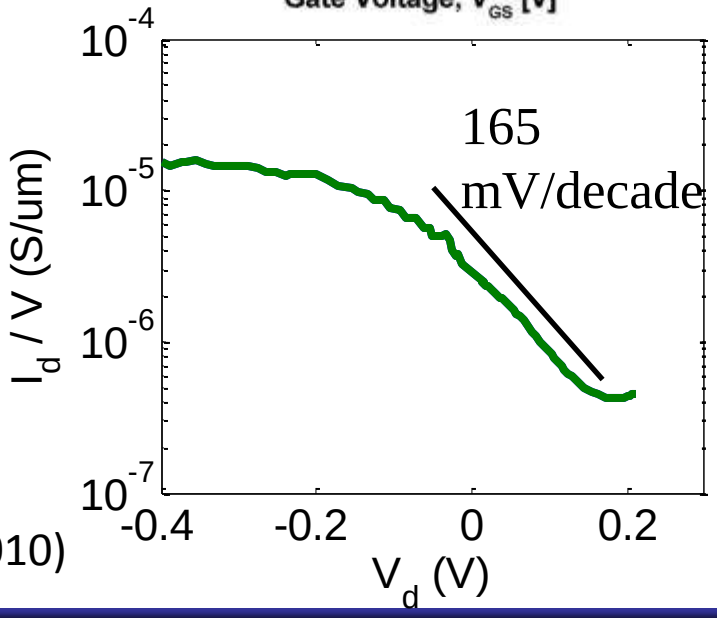


$In_{0.53}Ga_{0.47}As$ PIN Diode Characteristics Steeper than TFET!





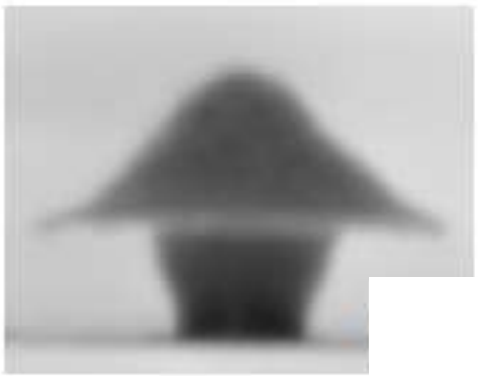


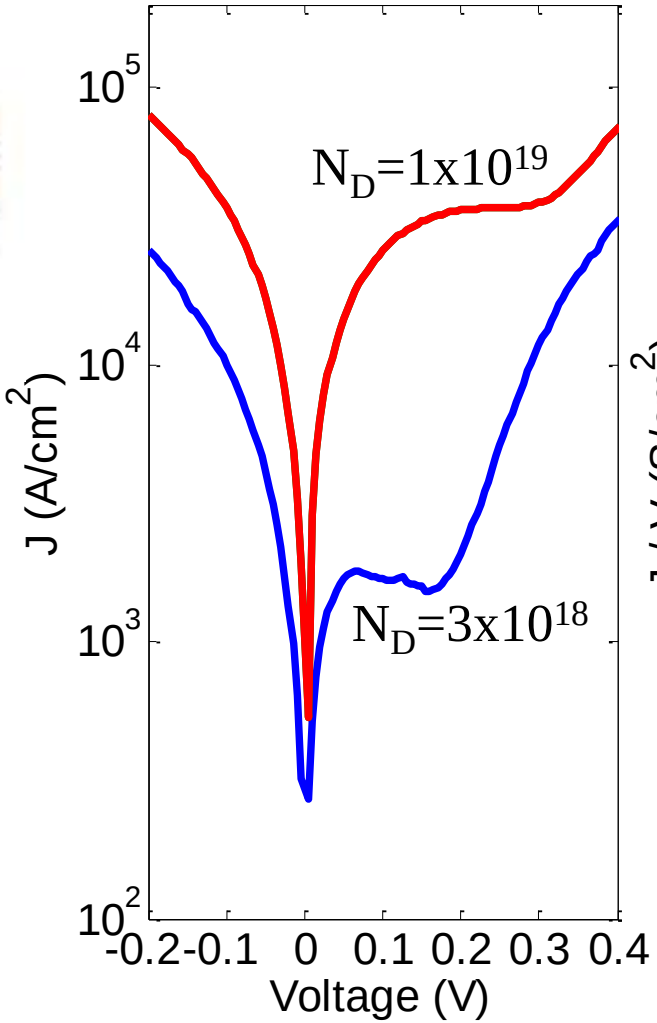


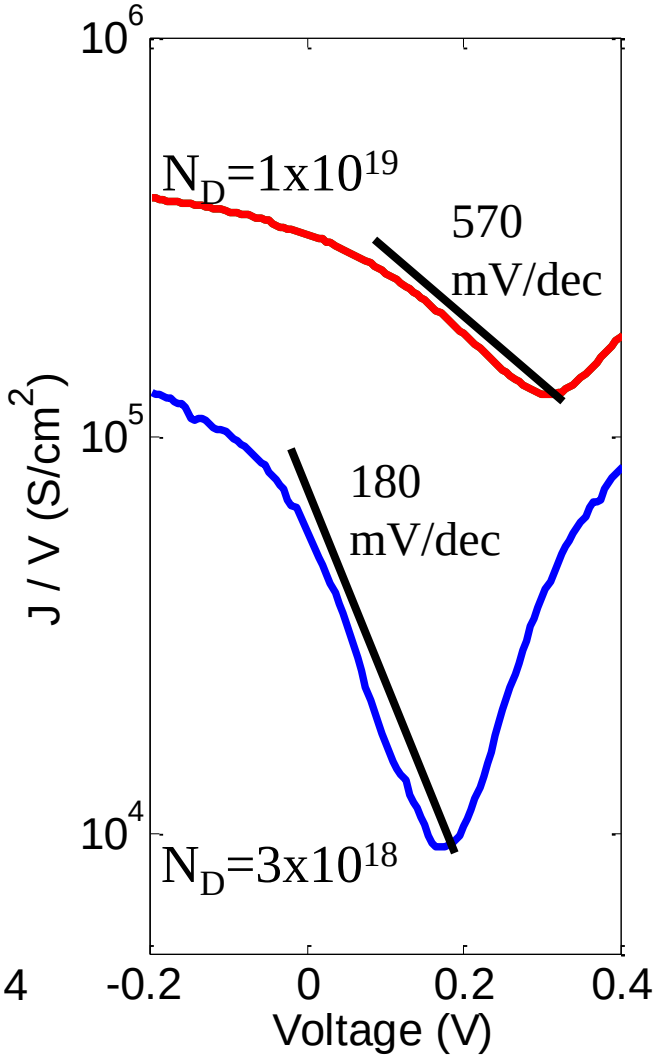
Mookerjea, (2010)

InAs Homojunction Diodes

$N_A=1.8x10^{19}$



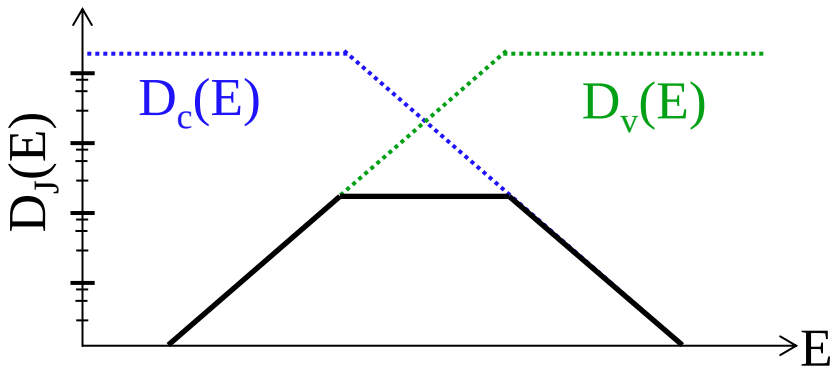




From Pawlik et all, "Benchmarking and Improving III-V Esaki Diode Performance with a Record 2.2 MA/cm2 Peak Current Density to Enhance TFET Drive Current" IEDM 2012, pp. 812-814

Modeling the Tunneling Current

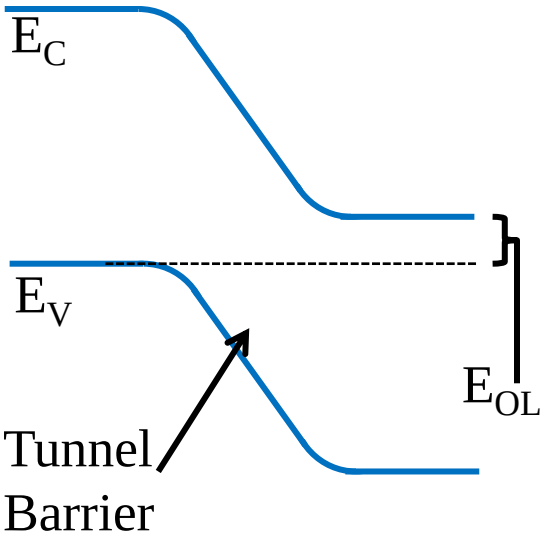
$$I \propto \int (f_C - f_V) \times T \times D_J(E) \times \partial E$$



$$I \propto e^{-|E_{OL}|/qV_0} \times \int_{E_V'}^{E_C'} (f_C - f_V) \times T \times D_0 \times \partial E$$

$$I \propto DOS \times \text{Tunneling Current}$$

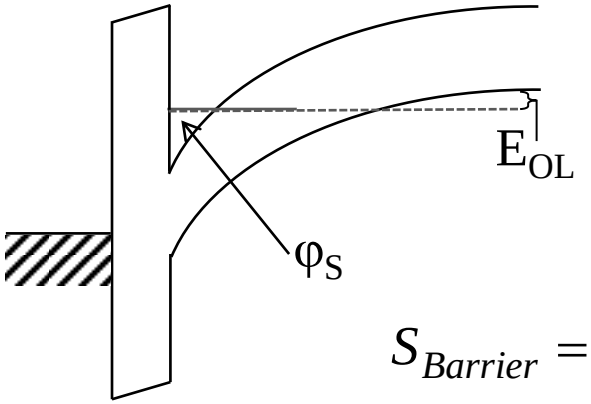
Four Factors Determine The Subthreshold Swing



$$I \propto DOS \times \text{Tunneling Probability}$$

$$SS = \left(\frac{d\log(I)}{dV_G} \right)^{-1}$$

$$= \frac{1}{\eta_{el}} \left(\frac{\eta_{conf}}{S_{DOS}} + \frac{1}{S_{Barrier}} \right)^{-1}$$



$$S_{Barrier} = \frac{d\log(T)}{d\phi_s} \quad S_{DOS} = \frac{d\log(DOS)}{dE_{OL}} \quad \eta_{conf} = \frac{dE_{OL}}{d\phi_s} \quad \eta_{el} = \frac{d\phi_s}{dV_G}$$

What is Happening in a Diode at Small Bias?

$$I \propto \int (f_C - f_V) \times T \times D_J(E) \times \partial E$$

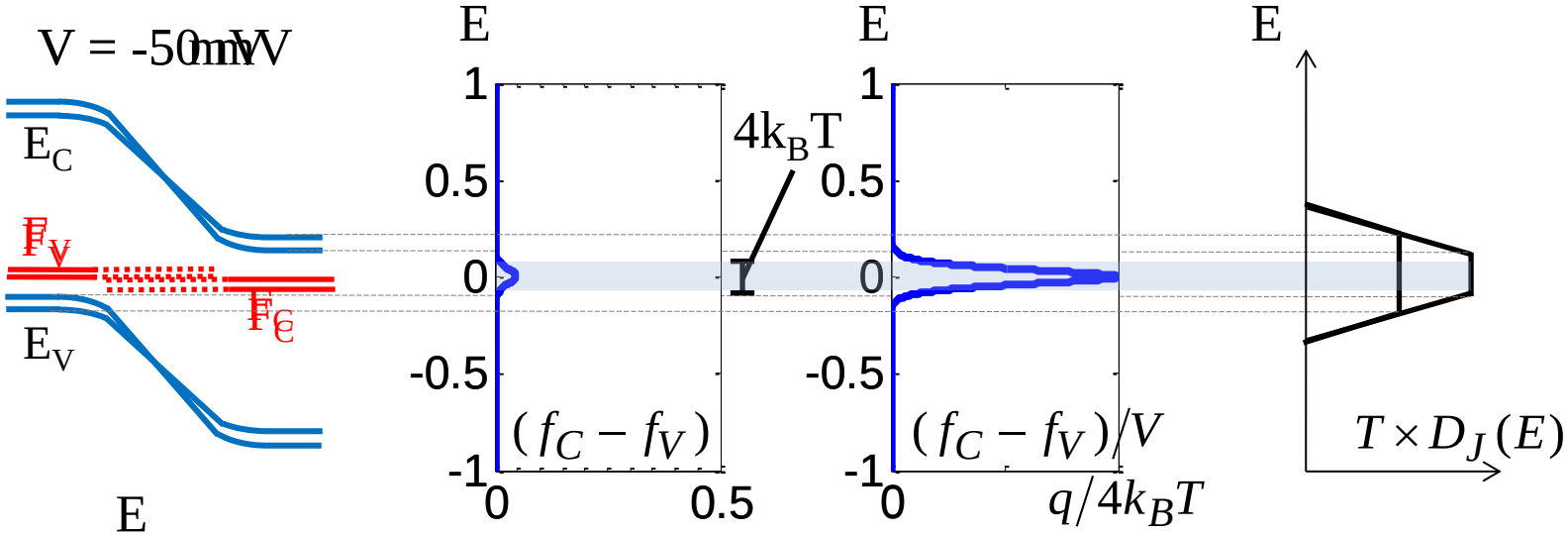
Fermi Functions Tunneling probability Joint Density of States

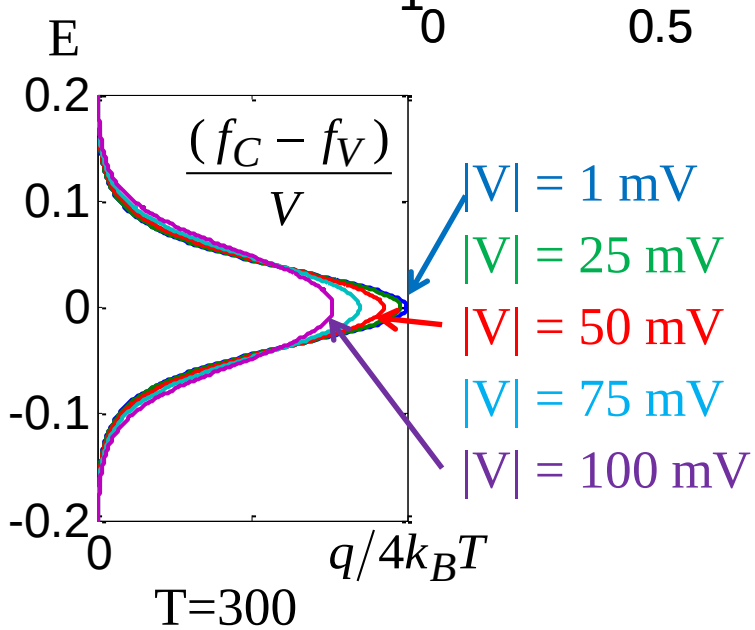
Consider Small Bias

$$I \propto \int (f_C - f_V) \times \partial E \times \frac{\int (f_C - f_V) \times T \times D(E) \times \partial E}{\int (f_C - f_V) \times \partial E}$$

$$= \quad qV \quad \times \quad \langle T \times D(E) \rangle \Big|_{-2k_{BT}}^{2k_B T}$$

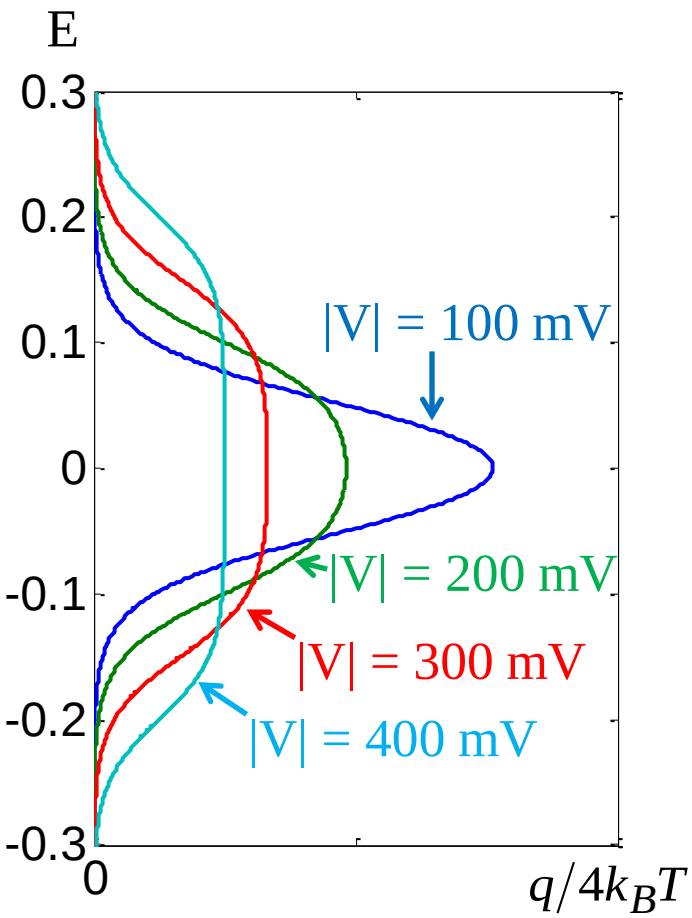
What is Happening in a Diode at Small Bias?





$$I \propto \quad qV \quad \times \quad \langle T \times D_J(E) \rangle \Big|_{-2k_BT}^{2k_BT}$$

What is Happening in a Diode at Large Bias > $4k_BT$?



$$(f_C - f_V)/V$$

$$I \propto \int (f_C - f_V)\partial E \times \frac{\int (f_C - f_V) \times T \times D(E) \times \partial E}{\int (f_C - f_V)\partial E}$$

$$= \quad qV \quad \times \quad \langle T \times D(E) \rangle \Big|_{-V/2}^{V/2}$$

Polycrystalline Silicon is Very Bad!

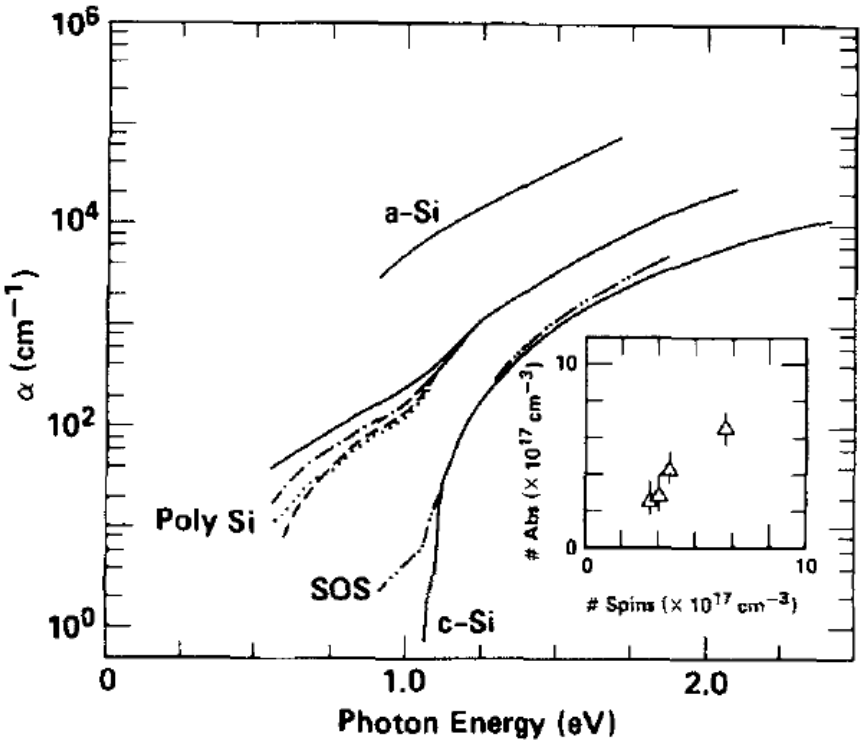


FIG. 1. Absorption vs photon energy for different intervals of atomic hydrogenation exposure. Evaporated amorphous silicon (*a*-Si) from Ref. 16. Fine grained polysilicon, unhydrogenated (solid), 60 min (dot-dash), 120 min (dash), 30 min (dotted), silicon-on-sapphire (SOS). Bulk crystallline silicon (*c*-Si) from Ref. 17. Inset shows the integrated density of optically absorbing defects with a cross section of 1.2×10^{-16} cm^{-2} (Ref. 8) vs the dangling bond spin density.

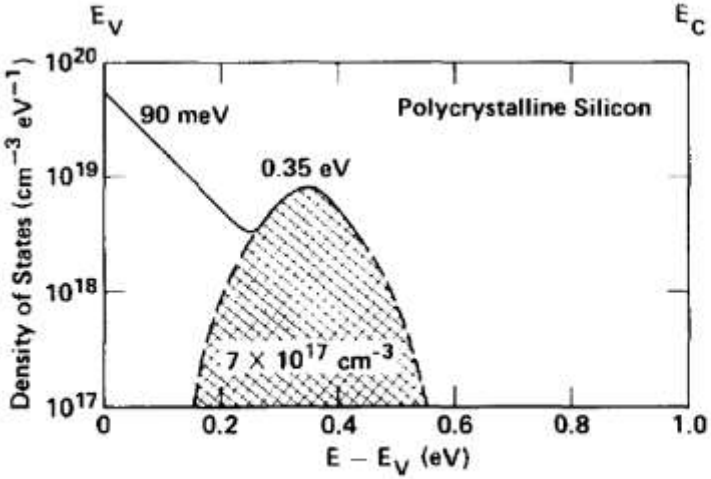
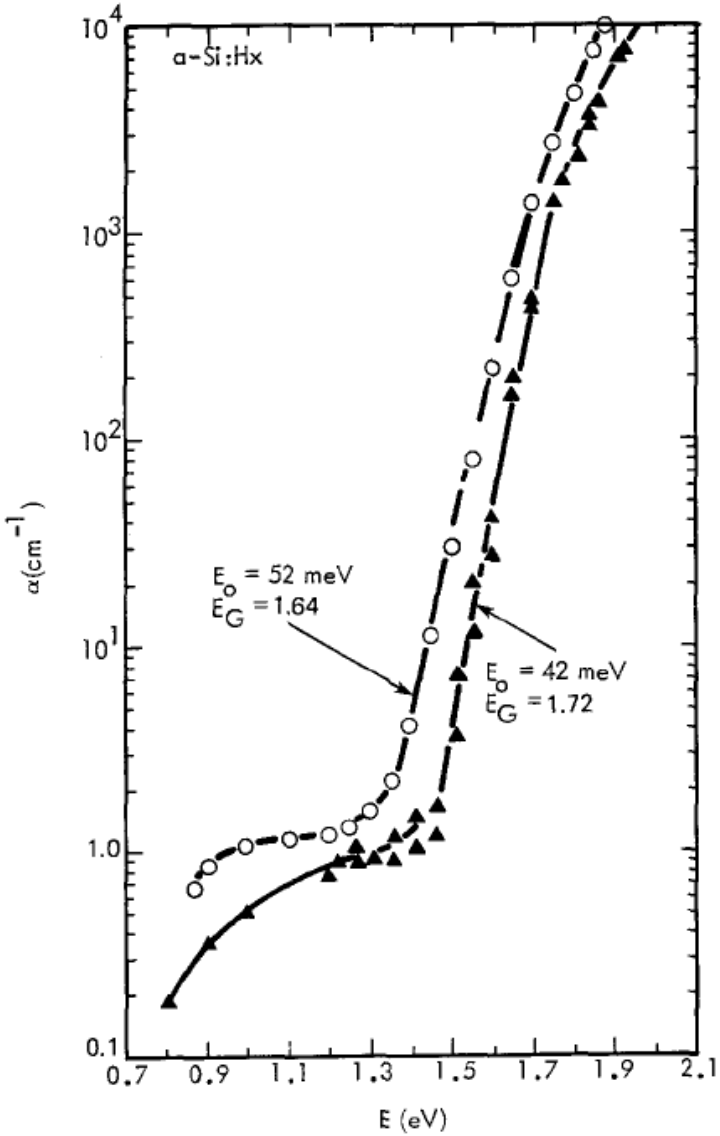


FIG. 3. Features of the grain boundary density of states derived from optical absorption and ESR measurements.

Jackson, Johnson and Biegelsen, "Density of Gap States of Silicon Grain boundaries Determined by Optical Absorption," 1982

Amorphous Silicon is Very Bad!



$$\alpha = \alpha_0 \exp[E - E_F/E_0(T, X)]$$

Fig. 1. Absorption edge of two films of amorphous silicon hydride (a-Si:H). The film with the higher Tauc gap was grown at a substrate temperature of 250°C compared with 200°C for the lower gap film. It has a hydrogen content of 14 at.% compared with 9 at.% for the lower gap film (adapted from ref. [2]).

Cody, "Urbach Edge of crystalline and amorphous silicon: a personal review" (1992)